Tektronix

Preliminary Service Information

11901 and 11902

Digitizing Oscilloscopes

Contents

Part 1
Theory of Operation

Preliminary

Theory of Operation

This section provides general and specific information on 11401 Digitizing Oscilloscope circuitry. The circuitry is grouped into functionally named modules that correspond to a specific circuit board (e.g., Main Processor or CRT Driver boards). In some cases, however, only the circuitry related to that board's function is discussed within that subsection.

The General System Description is presented first. This outlines the Digitizing Oscilloscope mainframe and describes instrument functions at a system level. Next is a Detailed System Description that divides each board into functional blocks. When reading these descriptions, refer to the system block diagram, the appropraite functional block diagram, and the appropriate schematics. Each block in the functional block diagrams corresponds to a subheading in the detailed theory descriptions. The detailed descriptions also provide schematic diamond numbers referencing the appropriate schematic.

Logic Conventions

Digital logic techniques are used to perform most functions within this instrument. Function and operation of the logic circuits are represented by standard logic symbols and terms. All logic functions are described using the positive logic convention. Positive logic is a system of notation whereby the more positive of two levels is the true, or 1 state; and the more negative level is the false, or 0 state.

In logic descriptions, the more positive of the two logic voltages is referred to as high, and the more negative state as low. The specific voltages that constitute a high or low state vary between different electronic devices (e.g., ECL and TTL).

Active-low signals in the text are indicated in the text by an (L) following the signal name, and a horizontal line above the signal name when on a schematic. Signal names without indicators are considered active-high. Hexadecimal numbers are identified with a *hex* suffix. Decimal numbers have no radix suffix.

General System Description

The Left, Right, and Center Plug-In compartments allow up to three plug-in units to be installed in the 11401 mainframe. Plug-in units are used to condition signals prior to delivery to the mainframe. These preconditioned signals are passed to the mainframe by two paths; 1) the Analog Input, and 2) the Serial Data digital interface.

Analog signals are directed through the Plug-In Interface board to the Acquisition and Time Base boards where they are changed into digital signals. The digitized signals are then stored in the Memory board RAMs. The Compressor board circuit extracts the stored digitized signals from the Memory board RAMs and conditions them for the Display Controller board circuit, where they are processed by the CRT Driver board and presented on the crt. The Compressor accomplishes this by squeezing the waveform into 500 points, which happens to be the fixed length (maximum number) of points that the Display Controller circuit can represent on the crt screen.

Digital signals pass through the Serial Data digitial interface which connects the Plug-In Interface board, via the Standard I/O board, to the Main Processor. The Serial Data bus is used for bi-directional control between plug-in s and the Main Processor, and for data communications.

The Main Processor communicates with the various circuit blocks through parallel Data and Address interface busses. The Serial Interface bus that connects the Display Controller circuit to the Rear Panel board is used for diagnostic purposes only.

Detailed System Description

Refer to the schematic diagrams while reading this Detailed Circuit Description. Complete schematic diagrams are provided at the rear of this manual.

Each diagram is divided into stages that are bordered with wide shaded lines. Further, each stage corresponds to a subheading in the Detailed System Description. The subheading also provides schematic diamond numbers that reference you back to the appropriate schematic.

Active-low signals are indicated in the text by an (L) following the signal name, and by a horizontal line above the signal name on the schematic diagrams. Signal names without indicators are considered active-high.

Assembly numbers (A numbers) identify components and the board these components are mounted on. The designation A7R200 identifies the board as assembly A7 (the Display Controller board), and the component number as resistor R200.

A2 Line Inverter, A3 Rectifierss, and Control 39

The Line Inverter, Rectifiers and Control circuits provide semi-regulated dc voltages to the Regulators circuitry. A schematic diagram of the Line Inverter, Rectifiers and Control circuitry is given on diagram 39, in Section II, Diagrams and Circuit Board Illustrations in Volume III of the service manual. The schematic is divided by gray shaded lines separating the circuitry into major stages. Sub-headings in the following discussion use these stage names to further identify the components and portions of the circuitry shown on diagram 39.

Line Interface

Power is applied through line filter FL99, line fuse F99 and POWER switch S130. The line filter FL99 prevents power-line interference from entering the instrument, and noise (in the range of one megahertz to one gigahertz) generated within the instrument from entering the line.

Resistor R99 serves to discharge the line capacitance in front of the line frequency bridge rectifiers and prevents a shock hazard from contact with the power connector pins when the power cord is disconnected.

The primary line fuse F99 prevents a fire hazard resulting from an improper setting of the 110/220 line switch, or from a major fault in the line-side circuitry. The thermal cutout switch S99 will disconnect the ac line power to the Line Interface circuitry when the heat sink temperature reaches approximately 75° C.

The principal power switch S130 disconnects both sides of the line. It is located on the rear panel and is not intended to be used as the primary means of turning the instrument on and off, as this function is handled by the Standby switch, located on the front panel.

Capacitors, C140 and C230, serve to bypass differential-mode noise, generated by the reverse recovery of the line-frequency rectifiers. Thermistors RT130 and RT240 limit the initial surge current when charging the line filter caps C200, C310, C200, C220 and C320. The thermal time constant of these thermistors is matched to the discharge time of the line filter caps, through bleeder resistor, R220. This ensures continued surge current limiting when the instrument is switched off and on several times in succession. Once the thermistors warm up they have negligible effect on the input current.

Spark gaps E231 and E230 prevent over charging the line filter caps C200, C310, C200, C220, and C320 due to improper setting of the 110/220 switch S250 or from high energy differential-mode line transients. CR340 operates as a full-wave rectifier, when S250 is set for 230 V operation, and as a voltage doubler, when S250 is set for 115 V operation, thus maintaining 230 to 380 volts dc across R220, for either setting of S250.

A neon flasher consisting of R640, C640 and DS640 indicates that hazardous voltages are present on the line filter caps. R220 discharges these capacitors in about two minutes. Transformer T440 provides the line trigger signal and power for the Standby Power circuitry, when the front-panel STANDBY switch is off and the rear-panel PRINCIPAL POWER switch is on.

Pulse Width Modulator

The primary means of controlling the output voltages from the Low-Voltage Rectifiers is the Pulse Width Modulator (PMW). The PWM transistors Q600 and Q601 are power MOSFET devices. They, in conjunction with L520 and CR500, form a negative buck switching regulator operating at a fixed frequency of 100 kHz. By controlling the conduction time of either transistor Q600 or Q601 the dc voltage applied to the 50 kHz Inverter (across C630 and C631) can be varied from zero volts up to the maximum voltage available across the line filter caps C200, C220, C310, and C320. Each of the PWM transistors conducts current on alternate switching cycles; they never conduct current at the same time. The control voltages for the gates of the PWM transistors are provided by T710. Resistors R600 and R610, and diodes CR600 and CR610 set the switching speed of the PMW transistors.

The 100 kilohertz variable-duty square wave developed at the drains of the PWM transistors is filtered by L520, C630 and C631. CR620 provides a path for the continuous dc current flowing in L520 when neither PWM transistor is conducting current.

Line Interface

Capacitors C520 and C401 provide a return path for common-mode current transients flowing in the chassis, caused by stray capacitive-coupling of the switching waveforms to the chassis. These capacitors also lower the impedance of the common mode noise sources within the mainframe and power supply. T410 further decouples these noise sources. The leakage inductance of transformer T410 (appearing as a differential-mode inductance to the PWM), in conjunction with C500, forces a continuous dc current to be drawn from the line storage caps C200, C310, C220, and C320.

Primary Current Sense

The primary current-sense transformer T700 samples the instantaneous current flowing in each PWM transistor. Q801 and Q800 clamp the secondaries of T700 to one base-emitter drop, giving true current-transforming operation. The current sense signal, +CS, is used to control the current flowing in the PWM transistors. It is used for both protection and feedback control.

50 kHz Inverter

The primary function of the inverter is to convert the dc voltage provided by the Pulse Width Modulator into a 50 kilohertz square wave. The 50 kHz Inverter MOSFET devices Q620 and Q610 are driven by a 10 volt peak, 50 kilohertz square wave from the gate drive transformer T720. Cross conduction (i.e. both transistors conducting at the same time) is prevented by R620, R611, CR621, and CR611 working into the gate-source capacitance of Q620 and Q601. During the 100 nanoseconds when neither transistor is conducting, diodes CR601 and CR620 provide a path for current from mutual inductances and leakage of the transformer. When the transformer primary current decays to zero, the respective MOSFET is biased on, ready to conduct. Thus no switching losses are associated with the half-wave bridge.

In the event of an inverter overvoltage condition, spark gap E630 will fire clamping the inverter input voltage to a safe level. If the over voltage is caused by a shorted PWM transistor, the spark gap will continue to conduct current until fuse F410 is opened and the inverter capacitors C630 and C631 discharge. If the over voltage condition is caused by an open

feedback path, the control circuit will limit the current to a level below that required to clear F410, and will then initiate a restart cycle, extinguishing the spark gap.

Rectifiers

Four separate sets of power transformer windings in T130 and T140 step the 50 kHz Inverter voltage down to the level required to generate eight semi-regulated outputs: ±54, ±17, ±7, ±5.2. Both power transformers operate in parallel but have different volt-second/turn ratio values in order to establish the proper output voltages.

After rectification and filtering, the semi-regulated outputs pass through current sense resistors, which are actually ECB (etched circuit board) traces tapped at specific lengths. The voltage across these traces is proportional to the current at the output terminals. These voltages (approximately 25 millivolts at the rated current) are used by the control circuit to limit fault currents in the mainframe plug-in units and to provide a diagnostic feature. The exception to this type of sensing is the ±54 V outputs, whose currents are sensed by R535, R636 and R637. The current sense signal is then level-shifted by Q530 and Q630.

Inverter Voltage Sampler

Components CR250, CR251, C251, R240, and Q250 form a sample-and-hold circuit that provides a voltage proportional to the inverter input voltage. This voltage provides feedback to the Error Amplifier circuit.

Ramp Injection

The Ramp Injection circuit consists of Q210 and associated components. The ramp signal is generated by charging C216 through R313. This voltage ramp is converted to a current by Q210, with R312 setting the magnitude of the injected current and, therefore, the current loop gain. The ramp generator is reset periodically by either the 100 kHz clock pulse or by the end of the PWM "ON" time, whichever comes first. (Normally the PWM signal, from U200A, pin 1 acting through CR200 and Q213 occurs first.) CR311 prevents the ramp capacitor C216 from discharging completely, leaving a small dc bias current in the ramp signal to hold off the converter during the power-up sequence.

Current Limit Comparator

The primary current sense signal plus the injected ramp current are summed and converted to a voltage by R305. The voltage across R305 (proportional to the instantaneous current in the PWM switching transistors) is applied to the current-limit comparator U410C. When the current in the PWM inductor L520 rises to a level determined by the error signal, the comparator resets the latch U200A ending the switching cycle. A new switching cycle is initiated by the 100 kHz clock pulse which sets the latch, turning "on" the alternate PWM transistor, until it is again reset by the current limit comparator. The error signal at the noninverting input to the current-limit comparator regulates the magnitude of current flowing in the PWM filter inductor L520 by controlling the on time of the PWM power switching transistors.

Error Amplifier

The +5.1S and +5I error signals are summed by the Error Amplifier U400B. The output terminal voltage is set by the +5.2 DC REF voltage, which is generated by U800 in the Local Power circuit and adjusted with potentiometer R800, 5.2 REF ADJ.

Soft Start

Shutdown of the converter is accomplished by ramping down the reference voltage input to the Error Amplifier. The RST(L) signal discharges the soft start capacitor C411 through CR313, Q410 and R324. All supplies will track this signal down to zero, where they will stay until the Fault Delay Latch (Diagram 40) times out. The RST(L) signal also pulls down the PFSET line, latching the PWRUP signal low and turning the Fault LEDs on for the duration of the time out.

After the 200 millisecond time out of the Fault Delay Latch, the clamp is removed from the 5.2 REF input to the Error Amplifier allowing the output voltage to rise at the rate determined by R323 charging the soft-start capacitor C411. The output voltages will track this rise, which has a time constant of approximately 10 milliseconds. After a delay of 20 milliseconds, as determined by the Power Fail Detect clamping network of R326, C323, CR321 Diag. 40, the power fail detect comparator U420D is reset, which turns off the LEDs and signals the mainframe that the output voltages are stable by activating PWRUP.

Standby Power

Components CR750 and C850 rectify and filter the secondary voltage of transformer T440 providing 17-30 volts to power the remote line switch and standby control. This voltage is regulated to 16 volts by a series-pass regulator composed of Q840, Q740, VR830, and associated components. Zener VR830 and divider R832-R833 are the positive and negative inputs to differential amplifier Q740. The output of the differential amplifier is the error voltage, and is applied to the base of the PNP series pass transistor Q840. Stability compensation is provided by C730.

When the power conversion circuitry is started, power is supplied by the inverter through the +17V line, acting through CR630. This shuts off Q840, unloading the line trigger transformer T440, which would otherwise cause distortion of the Line Trigger output (LTRIG).

Power is applied to the control circuit by grounding the DCPWRSW line, which turns on Q100. This is done by the remote power switch located on the front panel. Three-terminal regulator U300 sets the control circuit voltage to +12 volts.

100 kHZ Clock

When power is first applied the fault delay latch is set, preventing startup of the power conversion circuitry. Meanwhile, the 100 kHz clock pulse generator, made up of the comparator U410D and associated components, is allowed to stabilize. The frequency of the clock is set by R300 charging C301 to a voltage set by the divider R316 and R301. The pulse duration is set by C312.

Gate Drive

The 100kHz clock pulse toggles the divide-by-two flip-flop U200B. This provides the balanced 50 kilohertz drive signal for the 50kHz Inverter. U100 buffers both the PWM and 50kHz Inverter signals, providing sufficient current to drive the gate transformers as well as the Local Power charge pumps formed by CR110, CR111, CR112, CR113 and C212, C213, C214 and C215. These charge pumps establish the +22V and -10 V supplies. The input logic in Gate Drive U200 provides the alternating drive required by the PWM gate transformer. Damping and blocking are provided by R112-R111 and C120-C121, respectively. R201 and C200 create a time delay that holds the PWM latch U200A reset, when power is first applied.

Line Trigger

The line trigger signal is applied to the differential-to-single-ended amplifier U810A via the ±Uline signals. R730 and R736 set the output impedance and magnitude of the line trigger signal, LTRIG, (used by the mainframe and plug-in units) to less than 470 ohm and from 1 volt to 3 volt P-P, respectively.

Fault Detection 40

The Fault Detection circuit provides protection and diagnostics for the Regulators circuitry and the Line Inverter, Rectifiers and Control circuitry. The purpose of the protection circuitry is to prevent single faults in the power supply or mainframe power busses from becoming multiple faults. It does this by forcing an orderly shutdown of the power conversion circuitry, followed by restart attempts at regular intervals. Since all fault conditions have the same result, (i.e. shutdown of the converter) diagnostic features have been added to assist in locating the source and cause of the fault condition. A fault is identified as a persistent condition of excessive current, voltage or temperature in the power supply, mainframe, plug-in units or accessories.

A schematic diagram of the Fault Detection circuitry is given on diagram 40, in Section II, Diagrams and Circuit Board Illustrations in Volume III of the service manual. The schematic is divided by gray shaded lines separating the circuitry into major stages. Sub-headings in the following discussion use these stage names to further identify the components and portions of the circuitry shown on diagram XX.

Digital Current Sense

The overload fault sequence begins when the voltage drop across one of the Rectifiers current-sense trace resistances exceeds a reference level (about 25 mV) for several switching cycles (20 microseconds), tripping one of the current sense comparators (U610C, U610A, U610D, U610B, U410A, U620D, and U620B). The reference levels for the comparators are set by zener diode voltage divider networks (VR630, R635 and R630 is one example) which establishs the reference and, therefore, the current limit point for the +5.1 outputs.

Once tripped, the first action of a comparator is to pull down the PFSET (Power Fail Set) line, which is an analog "OR" of all the comparator outputs. This signal trips the Power Fail Detect comparator U420D turning on Q730, which pulls the PWRUP line down, signaling to the mainframe that a power failure is imminent. This signal also turns on the Fault LED Driver Q430, supplying current to all diagnostic LEDs via the LIGHTS(L) line. Meanwhile, the current sense comparator signal fires one of the PUT devices (for example Q721) which bypasses the LED current, extinguishing only the LED associated with the particular fault condition, while all other LEDs remain on.

Tripping the current sense comparator also begins a time delay, determined individually for the various outputs by discharging capacitor C324 through the individual resistors in the fault line (for example R513). During this delay, the LEDs are lit, the PWRUP signal is low and the power conversion circuitry attempts to clear the fault by providing maximum available power to the load. This time delay is approximately 0.1 millisecond allowing time to charge capacitors during transient loads. If the fault is cleared within this time, the LEDs are extinguished and the PWRUP line is brought high, resuming normal operation without disturbing the output voltages.

Analog Current Sense

The Analog Current Sense circuit operates in the same manner as described for the Digital Current Sense circuit.

Primary Current Limit Detect

The primary current is limited on a cycle-by-cycle basis by simply clamping the output of the Error Amplifier. VR300 does this by setting the peak current in the switching transistors. The zener clamp current flows through R303, turning on Q400, which, after a 10 millisecond delay, trips the Power Fail Detect and Fault Delay Latch initiating a converter shutdown.

Fault Delay Latch

If a fault persists, the fault Delay Latch, formed by C324 and the comparator in U420C, is set, pulling down the restart line, RST(L). This signal initiates shutdown of the power conversion circuitry, which will remain off for the duration (approximately 200 milliseconds) determined by C325, and C324 in series and R322 and R324 in parallel.

Fault LED Driver

This circuit completes the current path through Fault LED's DS533, DS630, DS530, and DS531. Transistors Q720, Q721, Q432, and Q431, respectively, determine which LEDs are illuminated.

Digital Voltage Sense

The Digital Voltage Sense circuitry detects over voltage and under voltage faults. The +5 and -5 volt supplies are sensed by VR700 and VR704, respectively. Exceeding the zener voltages causes Q700 and Q701 to turn on, tripping off the DIGVF indicator, DS533. A voltage fault of the post-regulated analog supplies is sensed by the Regulator circuit Voltage Fault Detect, whose output is OR'd with the Fault line by CR722 and CR721 to generate a restart.

Thermal Fault Sense

When inadequate air flow causes the thermal cutout switch S99 to reach 75° C, an over-temperature condition occurs interrupting the dc input to the PWM. The converter shutdown will continue until the sensor has cooled to 50° C, only then initiating a restart cycle.

Power Fail Detect

Power fail detection is accomplished by monitoring the duty cycle of the pulse-width modulator (PWM). The PWM(L) signal is converted to a dc voltage by the integrator formed by R328, R320, R327, C320 and C321. Since the input to the integrator is an inverted PWM signal, the dc output of the integrator is directly proportional to the rectified AC line. When this voltage drops below a level set by divider R330 and R329 (corresponding to a duty cycle of 95%), the comparator U420D pulls down on the PWRUP signal, and lights all diagnostic LEDs. Power conversion continues until an under voltage condition is detected, giving the mainframe time to prepare for a power failure. Once the rectified line voltage has dropped below the minimum regulation range (190 Vdc), the converter is shut down by the under voltage detect circuit leaving a substantial stored charge in the line storage capacitors, thus preventing large surge currents when the ac line is reapplied with the thermistors still hot.

Fan Speed Controller

Transistor Q640 and associated components comprise the fan speed modulator. A 10 hertz pulse-width modulated signal from the fan speed controller (FAN PWM) sets the dc fan speed by pulsing it on, then allowing it to freewheel through diode CR740. Fuse F740 protects these devices from any faults on the fan circuit.

The fan speed controller, made up of U730, U710B, and associated components, functions as a limited range feedback control system, which attempts to keep the temperature of the exit air stream constant over the specified operating range of ambient temperatures. The exit air temperature is sensed by U730, and is converted to a dc voltage (VTEMP) by R732. This voltage becomes the reference for a 10 hertz pulse width modulator formed by the operational amplifier U710B. The frequency of oscillation is set by C821, which, with R728, serves as an integrator, converting the fan output back into a dc voltage, which is compared to VTEMP. The

action of the circuit is to maintain the two voltages at the same average dc level. When a temperature rise is sensed by U710B, the pulse width to the fan is increased, speeding it up, which in turn reduces the temperature of the exit air, maintaining closed-loop control.

A4 Regulators 41

The Regulators convert semi-regulated voltages into stabilized low-ripple output voltages. A schematic diagram of the Regulators is given on diagram 41, in Section II, Diagrams and Circuit Board Illustrations in Volume III of the service manual. The schematic is divided by gray shaded lines separating the circuitry into major stages. Sub-headings in the following discussion use these stage names to further identify the components and portions of the circuitry shown on diagram 41.

Local Regulator Power

The operational amplifiers used for the +50, +15, +5, –50, –15 and –5 volt Regulators require that the following special voltages be generated for their operation:

(1) The +20 volt supply is generated from the semi-regulated +54 volt supply by reference zener diode VR732.

(2) The –20 volt supply is generated from the semi-regulated –54 volt supply by reference zener diode VR720 and transistor Q820.

(3) The +10 volt supply is generated from the semi-regulated +54 volt supply, by zener diode VR730.

(4) The –10 volt supply is generated from the semi-regulated –54 volt supply by zener diode VR731.

(5) The +10.0 REF is used as a reference voltage.

+50 V Regulator

Semi-regulated +54 volts from the Line Inverter, Rectifier and Control circuit (diagram 39) is the unregulated voltage source for this supply. Differential amplifier U220C compares the feedback voltage at pin 9 against the reference voltage at pin 10. The error output at pin 8 of U220C reflects a difference between these two inputs. A sample of the +50-volt output is connected to U220C pin 9 via divider network R241 and R235. Notice that the feedback voltage of this divider is obtained from a line labeled +50S (sense). If the feedback voltages were obtained at the supply, the voltage at the load would not stay constant, due to the voltage drop across the resistance of the cable between the supply and its load. The separate sense line overcomes this problem by sensing the voltage at the load. Because the current in the sense line is small and constant, the load voltage is held constant regardless of the load current.

Regulation of voltage occurs as follows: If the +50 V Regulator output decreases (becomes less positive) due to an increase in load or a decrease in input voltage (as a result of line-voltage change or ripple), the voltage across divider R235 and R241 also decreases. This results in a less positive level, at pin 9 of U220C, than that established by the +10.0 REF supply at pin 10 of U220C. This decreases the current through VR510 causing an increase in current through the base-emitter junction of Q501. The result is increased conduction of Q501, the series regulator device. The load current increases and, therefore, the voltage across the load also increases sufficiently to balance the input to the differential amplifier U220C. The REF ADJ, R830, on the +10 Ref supply sets the output level of this supply.

-15 V Regulator

Basic operation of in the -15 V Regulator is the same as for the +50 V Regulator. The reference level for this supply is established through R130 at pin 12 of U230D. The divider ratio of R122 and R135 sets a level of zero volts at pin 13 of U230D. Any change at the output of the -15 volt supply appears at pin 13 of U230D as an error signal. The output voltage is regulated in the same manner as described for the +50 Regulator. Diode CR433 will keep the output of this supply from going more positive than about -4.4 volts if it gets shorted to one of the more positive supplies.

+5 V Regulator

The operation of the +5 V Regulator is basically the same as described for the previous supply regulators. Error voltage is provided through R134 to pin 6 of U230B, and pin 5 is referenced to the +10.0 REF supply. The divider ratio of R138 and R139 is 2:1, so pin 5 of U230B is at five volts when the supply is operating normally. Any change at the output of the +5 V Regulator supply appears at pin 6 of U230B as an error signal. Diode CR431 limits the output of this supply to about -0.6 volt, if it gets shorted to one of the negative supplies.

+15 V Regulator

The +15 V Regulator operates in the same manner as the +50 Regulator. Error feedback voltage to pin 13 of U220D is provided through R236. Pin 12 of U220D is referenced to the +10.0 REF supply. The divider ratio of R237 and R236 sets pin 13 of U220D at +15 volts. Any change in the output level of the +15 V Regulator appears at pin 13 of U220D as an error signal. This results in an opposite change at the output, pin 14 of U220D, which is conveyed to the series regulator transistor Q400, through Q311, to correct the error in the output voltage of the supply. Diode CR420 limits the output of this supply to about 4.6 volts if it gets shorted to one of the negative supplies.

-50 V Regulator

Operation of the -50 V Regulator is basically the same as described for the +50V Regulator. Error voltage to pin 9 of U230C is provided by divider R224-R223 and is referenced to the -50S (sense) line. The divider ratio of R224 and R223 sets the level at pin 9 of U230C to zero volts when the output of this supply is correct. Protection diode CR432 limits the output voltage of this supply to -14.4 volts should the supply be shorted to a more positive supply.

Voltage Fault Detect

Over-voltage or under-voltage of any regulated supply is detected by the window comparators U220A, U220B, and associated resistors. These resistors set a hysteresis window that is 5% of the regulator sense line voltages. The output of the comparators is analog "OR'd" and sent to the Regulator Fault Indicator circuitry on the Control Rectifier board, where the signal is latched into an LED indicator and initiates an immediate shutdown of the entire power supply.

A5 Acquisition Board

Sampling Hybrid/Vertical Channel Select

The Sampling Hybrid contains three sampling modules and a four input channel switch. The Sampling Hybrid simultaneously samples the vertical signal from each plug-in compartment. The differential outputs of the three samplers are connected to the Channel Switch IC. The Channel Switch IC converts the differential sampled signal to a single-ended signal and provides a means to select each sampled signal for ouput to the A/D converter. A calibration voltage(CHSWREF) used for A/D auto-calibration is also connected to the fourth channel switch input.

The Timebase board provides signals(VS0, VS1) to the Vertical Channel Select circuitry that control the Channel Switch output.

Strobe Driver/Sample Gate Generator

The Strobe Driver IC provides the differential sampling strobes to the Sampling Hybrid. The Sample Gate Generator creates the sampling pulse from the falling edge of SAMPLECK(20MHz). SAMPLE_ENABLE prevents sample pulses from occurring while the A/D converter sequentially digitizes the simultaneously sampled plug-in signals.

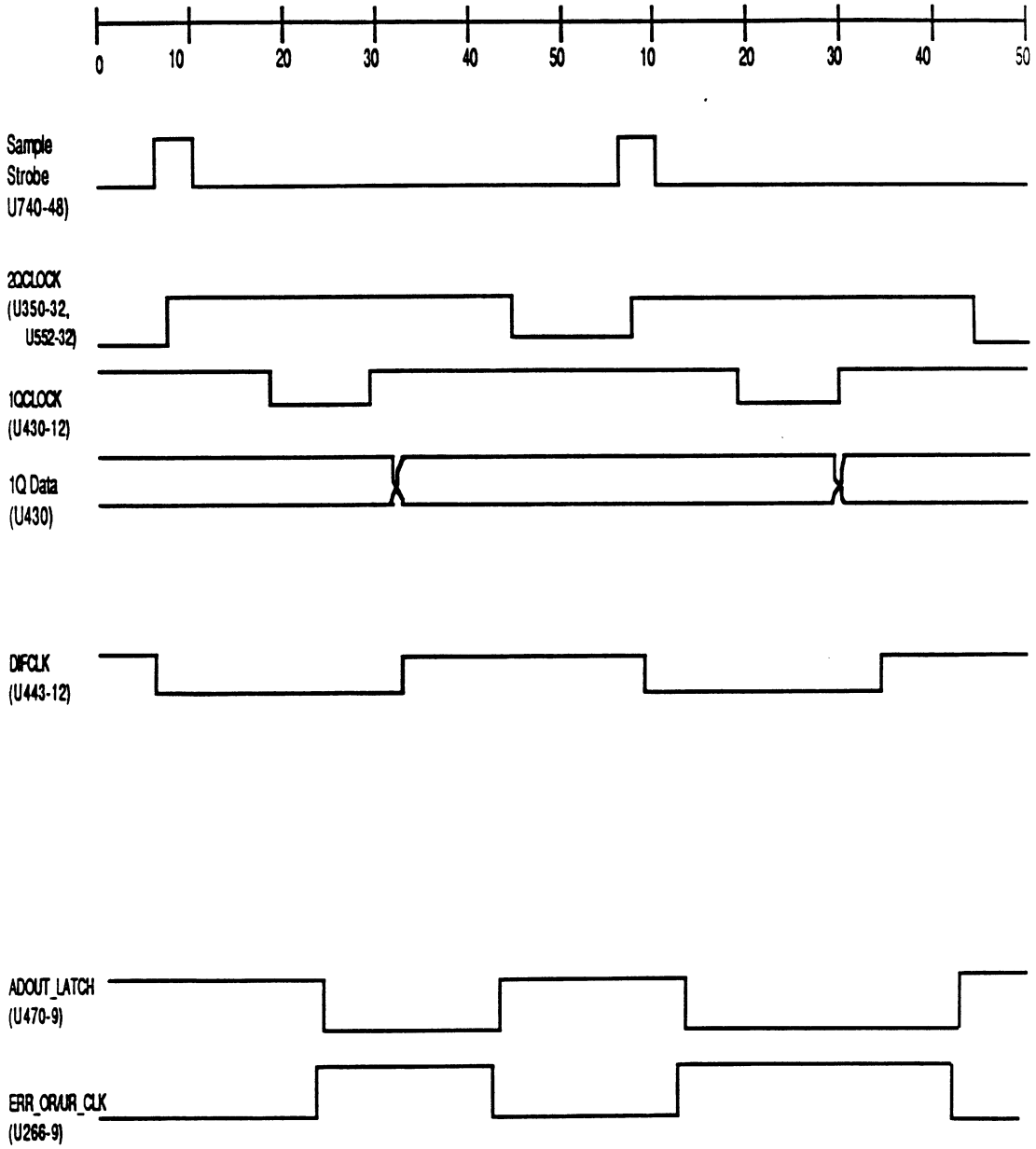
A/D Converter

The A/D converter converts the sampled signal to a 10 bit digital value. The A/D converter is a two stage flash with error correction. The output of the first stage 5 bit A/D converter(U430) is converted to an analog voltage by the 5 bit DAC(U442) and subtracted from the sampled input signal by the Difference Amplifier(U443). The output of the Difference Amplifier is applied to the second stage which uses two stacked 5 bit A/D converters(U350, U552) to yeild a six bit A/D converter. The upper and lower 16 codes of the second stage are used for error correction that can correct for errrors in the first stage conversion. The Error Correction PROM corrects the LSB of the first stage when an error is sensed by the second stage. The Over/Under Range Logic(U266) defeats error correction when the magnitude of the input signal is greater than full scale.

Clock Generator

The Clock Generator circuitry receives the 200MHz clock from the PLL and uses a twisted ring shift register counter (U810, U712 and U710) to generate the 20MHz clock. Each successive tap of the shift register generates a 20MHz clock that is delayed 5ns.

The Clock Generator provides 20MHz clocks to the Sample Gate Generator and the first stage, second stage and output latches of the A/D converter. Also provided are the 20MHz clocks for the Coarse Time Interpolator, the serial data out shift register of the Fine Time Interpolator and the Master Clock(MCK) for the Timebase Board. Figure xx2 illustrates the clocks generated for the sampler and A/D.



Trigger

The Trigger Hybrid(U1710) receives and processes analog signals from the left, center and right Plug-in compartments. Two identical ICs within the Trigger Hybrid output trigger gate signals which are used by the Main and Window holdoff, time interpolation and acquistion circuits.

The microprocesser serially loads data to onboard shift registers which control the selection of coupling, slope and free run via U1710-48. A separate serial load clock is provided for the Main and Window shift registers at U1710-23 and U1710-47 respectively. Main and Window trigger source data is serially loaded and latched into U2030.

Main Trigger Holdoff

The Main Trigger Holdoff circuitry limits the rate at which trigger gate signals can be generated and provides the user a means to trigger on the desired portion of a complex signal. Figure xx1 illustrates the interaction between the holdoff signal and the Main Trigger Gate(TGM). The Trigger Hybrid(U1710) drives the Main Trigger Gate output high when the input signal crosses the user selected trigger level input. The Trigger gate remains high until the Main Holdoff circuit times out and then resets the Main Trigger gate. Trigger signals are rejected by the Trigger IC when the Trigger Gate is high or MTHO is high.

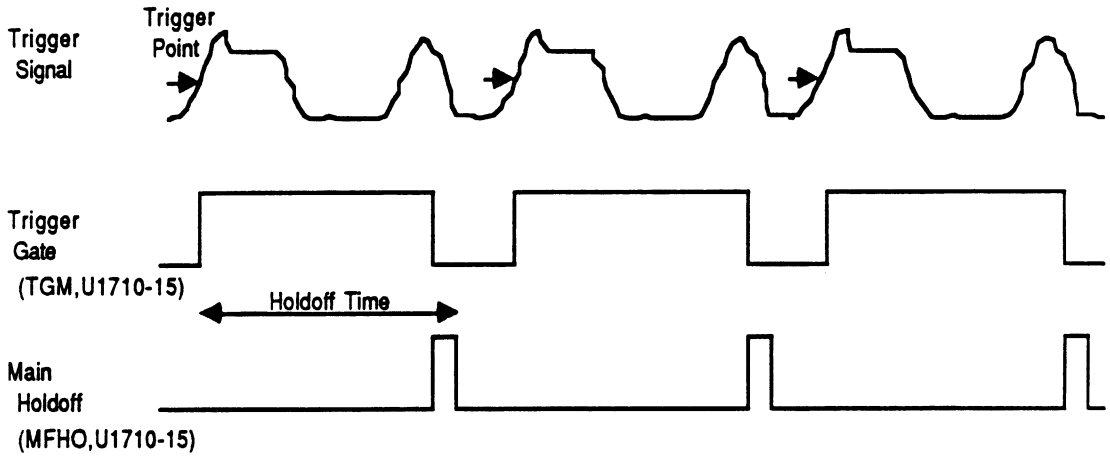


Figure xx1

The Main Holdoff circuitry is comprised of a coarse and a fine section. The coarse section contains a digital counter(U264), and and circuitry to generate the holdoff pulse. The coarse holdoff circuits are clocked from the 19.6608MHz clock.

The Trigger Gate is synchronized to the 19.6608MHz clock via U1546A and U1546B. Upon receipt of this synchronized trigger gate(U1546-9), the digital counter begins counting down the holdoff interval. When the digital count is completed, /MHORESET is asserted low which places the counter in the load state and also starts the holdoff pulse. The holdoff pulse (HOPULSE) is generated by a the Holdoff pulse shift register comprised of U1550 and U1644. The input to the shift register(U1550-3) is set to a high for normal operation. Thus following the reset of the shift register by /MHORESET, a high is clocked through to the output by the 19.6608MHz clock. When the holdoff interval is longer than 500usec, the falling edge of HOPULSE resets U1832B and causes MFHO(U1832-9) to go low and thereby enables the Trigger IC to produce another trigger gate.

The first tap of the Holdoff pulse shift register enables circuitry(U1352, U1552, U1554B) which creates signals that arm the events counter, the record trigger and window holdoff circuits.

Main Fine Holdoff

The Main Fine Holdoff circuitry is used in conjunction with the digital holdoff to increase the main holdoff resolution to minimum of 500ps. Analog ramps are used to remove the uncertainty between the trigger and digital holdoff clock.

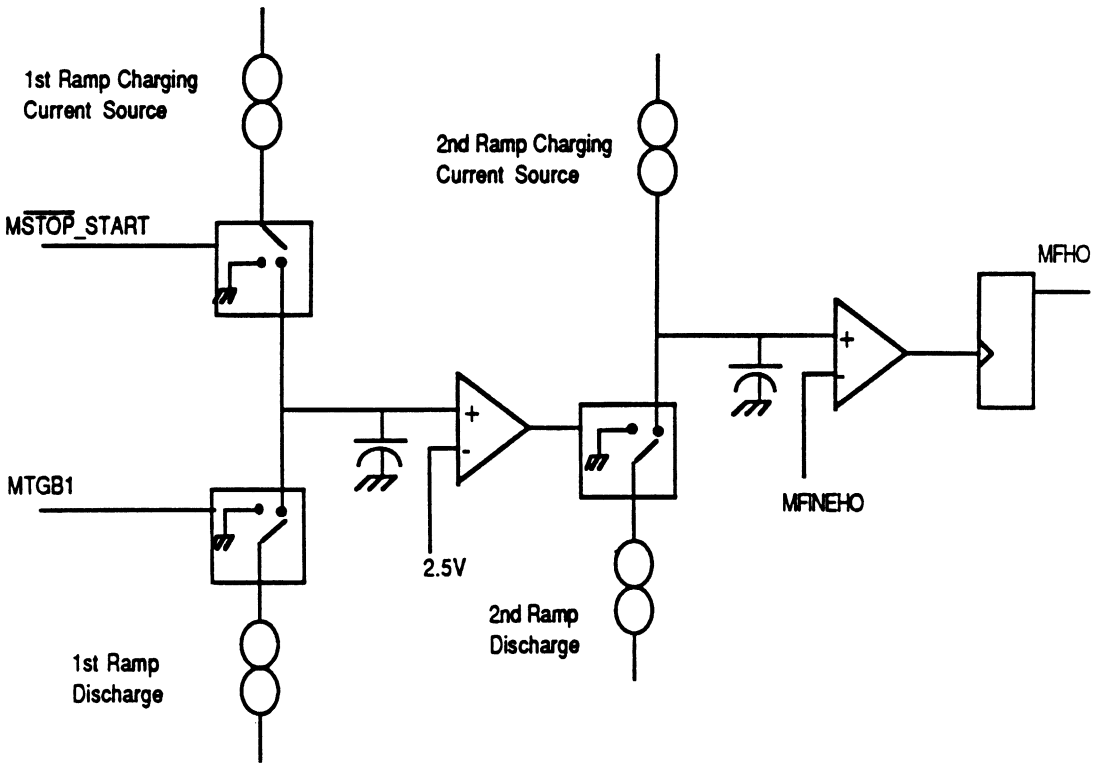
A positive going analog voltage ramp begins when the Main Trigger occurs and stops on the second holdoff clock edge following the trigger.

Since the holdoff clock occurs randomly with respect to the trigger, the time that the analog ramps runs will vary. Therefore the voltage at which the analog ramp stops is a measure of the time between the trigger and the holdoff clock.

The voltage that the ramp stops at is stored on a capacitor until the digital holdoff count is complete and then the ramp begins again. The ramp runs until it crosses a fixed comparison voltage that is set one input of a voltage comparator(U1940A). The voltage ramp is allowed to run long enough to make up for propagation delay variations in the digital holdoff circuitry. U1940A makes a positive transistion when the ramp crosses the fixed comparison level. The time between the trigger and the positive transistion of the voltage comparator is constant.

Another analog voltage ramp begins at the positive transistion of the voltage comparator and the first ramp is reset to it's start position.

The second voltage ramp runs until it crosses the comparison voltage set on a second voltage comparator(U1940B). This comparison voltage is varies via software control to allow the positive transition of U1940B to vary up to one holdoff cycle(50.86ns) in 500ps steps.



Delay by Events

The Delay by Events counter allows the acquistion of the Window record to be delayed relative to the Main trigger point by a user specified number of events. The Delay by Events counter is made up of three sections. The first two high speed sections reside on the Acquistion Board and a low speed section is contained within U264 on the Timebase Board.

When Delay by Events is selected, the Window Trigger IC ignores the window holdoff input(U1710-39) and performs as a high speed comparator. When the window trigger signal is above the trigger threshold the trigger gate(TGW) is high and vice versa. The first stage of the Events counter(U1530) is a 2 bit shift register counter which is clocked by TGW. The first stage output(U1530-15) clocks the second stage 4 bit counter which in turn clocks the slow counter(U264) on the timebase board. After each stage has reached terminal count, a clock signal will be generated on the next positive transistion of TGW which sends a differential trigger signal to the Window Time Interpolator via U1420A.

Time Interpolators

The Time Interpolator measures the time between the trigger signal and the sampling strobe once during each acquistion cycle. Separate Time Interpolators measure the trigger to sampling strobe time for the Main and Window triggers. Each Time Interpolator consists of a coarse and a fine section.

The coarse measurement begins when the /MSFR output of the Main Fine Time Interpolator makes a negative transistion. This occurs following the Main Trigger and enables the 200MHz clock to pass through gate U1110B to the coarse counter(U922). The coarse counter counts until the sampling strobe(via U1010-14) occurs, yeilding the trigger to strobe time with 5ns of resolution. The Main Coarse Counter is intialized before each acquistion cycle via the Coarse_LD_CK and Coarse_LD signals generated in the holdoff circuitry. The Window Coarse Time Interpolator operates in the same manner.

The Fine Time Interpolators measure the time between the trigger and the 200MHz clock with 10 ps of resolution. The measured time is converted to a digital count within the Fine Time Interpolator and is serially shifted into the Fine Time Interpolator Shift Register when the measurement is complete. The data from the Main and Window Fine Time Interpolators is serially multiplexed to the DAG IC on the Timebase board.

Upon receipt of the Fine Request(/FRQ) signal from the Time Interpolator circuitry the DAG IC reads the Main Coarse and Fine data from the coarse multiplexer(U1244, U1246) and the fine multiplexer(U1250) respectively. After the Main data is read the coarse multiplexer input is switched to the Window coarse data and the Fine Time Interpolator Shift Register is loaded with Window Fine data upon receipt of the Fine Acknowledge(/FAK) signal from the DAG IC. The Window data is then loaded into the DAG IC.

ACQ Autocal & Refresh

Diagram 12

This diagram contains the circuitry for automatic calibration of various digitizer circuits, including the acquisition, time base, and trigger circuits. It also contains circuitry for analog voltage refresh of various digitizer circuits, including the trigger level and holdoff, acquisition time interpolators, two-stage A/D flash converter, and sampling circuits.

Voltage Reference DAC

The DAC (U1470) provides multiplexed analog output of various refresh voltages to the analog sampling bridges: Refresh Bank 1 (U960 and U970), Refresh Bank 2 (U1270 and U1272), and Refresh Bank 3 (U1072 and U1170). The microprocessor writes a digital input value to the DAC every 400 microseconds. Each digital input value represents a unique reference or control voltage needed for one of the circuits listed in the paragraph above.

The DAC's Offset (R1576) and Gain (R1582) settings are adjusted during diagnostics calibration initiated at the front panel (see the 11401/11402 Service, Vol.1, Diagnostics manual for details).

Refresh Banks 1, 2, and 3

After the DAC presents the analog voltage to the sampling bridges of the refresh banks, the microprocessor places an address at the input of the addressable latches (U1070, U1370, and U1172). Then the not-SCAN signal from pin 34 of J84 enables the input address to select the addressed output which will follow the level of the D input (starting with Refresh Bank 1). This, in turn, selects which switch of the sampling bridge that closes for 400 microseconds (all analog switches of the sampling bridge are initially open). Thus, the analog voltage from the DAC is stored on the capacitor of the now closed refresh bank sampling bridge switch. This voltage is then passed from the high impedance output buffer (of the closed switch) to the circuit it supplies the reference or control voltage for. This process is repeated every 400 microseconds, starting, sequentially, with each switch of Refresh Bank 1; then, each switch of Refresh Bank 2; and, then, each switch of Refresh Bank 3, so that each reference or control voltage circuit is continually refreshed with the appropriate voltage.

Cal Select

During the plug-in calibration mode, register U1570 receives an address from the microprocessor that indicates the appropriate settings for the Calibrator and plug-in calibration signals. The not-CALRANGE signal from pin 26 of J84 clocks in the specified mode settings. In particular, pin 19 of U1570 drives the enabling of either the 450 Ω or 50 Ω output impedance for the Calibrator signal and decoder U1670A&B provide the appropriate enables for the Cal Gain Select stage.

Calgain Select

A digital value from the microprocessor provides an analog plug-in Calibrator Voltage Reference of, typically, 5 to 10 volts from the DAC and Refresh Bank 2 circuitry to the input amp of the Cal Gain Select stage, which attenuates the voltage. Analog switches in U1672, in conjunction with part of resistor divider network R1877, provide X1, X2, or X4 attenuation and analog switches in U1772, in conjunction with part of resistor divider network R1877, provide attenuation of X1, X10, X100, or X1000, depending on the decoded signal from the Cal Select stage. The voltage is then passed to the Calibrator Output Buffer stage.

Caloutput Buffer

Op amp U1870, with transistors Q1968 and Q1969, drive the calibrator output signals, including Plug-in Cal at pin 3 of J91A and Front Panel Cal to the CALIBRATOR output.

Front-Panel Calibrator

The front-panel CALIBRATOR signal is either a dc reference level of about 6 millivolts to 6 volts for probe calibration of gain and offset; or a 6 volt, 1 kHz or 2 MHz square-wave for probe compensation and deskewing. The square-wave is generated by Q1668, Q1562, Q1560, and their associated circuitry whenever the ???? circuit enables the CAL_ CLK signal into flip-flop U2060A (this happens during the probe deskewing and compensation operations). The output impedance for the CALIBRATOR is, again, either 450 ohms or 50 ohms, depending on the type of 11000-series probe attached to the bnc.

Plug-in Ground Select

Demultiplexer U1970 receives an address from the Cal Select circuit (U1570) that indicates which plug-in compartment is selected. Appropriate ground reference currents from the plug-in and the front panel are passed from op amp U1870B to the front-panel and plug-in cal circuitry to offset any voltage difference.

A6 Time Base Board

The basic function of the time base controller (A6 Time Base board - diagrams 13 through 20) is to use the acquistion system to produce waveform records of a desired length and resolution at a specified position. Because of the high-speed operations required of the time base system, the time base controller makes entensive use of hardware circuits that are optimized for this purpose. An Intel 80186 microprocessor (U224 - diagram 16) provides a means of setting up the hardware for most modes of operation, although, in a number of cases, a software approach must be used to handle complex functions. The microprocessor uses 16k bytes of RAM (U281 & U283 - diagram 16) and 128k bytes of ROM (U271 & U273 - diagram 16), along with many I/O devices, to accomplish numerous functions. However, in normal operation, the time base system may operate completely independent of the microprocessor for many acquistion and transfer cycles, as the hardware will restart itself at the end of each cycle, unless instructed to do otherwise by the microprocessor.

Before we can talk about the operation of the time base system, we need to understand what a record is and what parameters and constraints are associated with it. In a conventional oscilloscope, the trigger point on the displayed waveform is very near the start of the sweep. While, in a digital scope, such as the 11401/11402, it is possible to position the trigger point anywhere relative to the record, however, the trigger point for the main record must occur during the main record. This can be at the beginning or at the end of the record, or anyplace inbetween. This can complicate matters, somewhat, since this means that, in effect, we have to know where the trigger is before the data is acquired so that we can acquire enough data before the trigger point to complete the record. By setting up a counter to count from the beginning of the sweep to a value which is equal to the time before the trigger, we can collect enough points before the trigger. Once the trigger has occurred, we can count the amount of data that occurs after the trigger to collect the proper number of points. Then, we need only count back the required number of points (as calculated by the Destination Address Generator, see U166 - diagram 20 and the overview description, below, for more details) from the end of the acquired points to identify a complete record.

So far, this dicussion has centered on the main record. In the 11401/11402 system, we also allow two window records to be defined by the user, with the constraint that they must have at least one point in common with the main record (this is mainly to let the user see where the window really is). The window records' use a single trigger source, but their trigger is not confined to being on the window record. The window trigger, in most cases, is connected to the main trigger system via hardware located on the acquistion board. In that case, the windows are positioned relative to the main trigger point, but because of the above contraints, the main trigger does not have to occur during the window records. So, it is possible to have a window that is completely before or after the main trigger. These requirements cause the hardware within the time base system to be used in several different manners for different sorts of setup conditions.

Note that when looking at the time base system, one must also consider the acquistion board, as the two boards are very interelated in their functions. In fact, in many cases, a function may be split between the two boards in order to take advantage of each's strengths.

Functional Overview

Operation: I will try to indicate the events that happen during a normal acquistion cycle. Please keep in mind that this not an inclusive list for all conditions, but a simple case that we can build on.

The starting point for the system is the occurrence of the RESTART signal, this may be created due to the previous cycle finishing or by the microprocessor starting the digitizer system. The occurrence of the RESTART signal causes a number of things to happen: the acquistion memory system will switch into the acquistion (write) mode and the time base logic will intialize for the next sweep. The time base logic starts the PRETC counter, which is used to guarantee that at least the required number of pretrigger points will be acquired before the trigger. With this, the rate counters for the main and window time bases will begin to output time base requests. It it important to note that the rate counters both run continously, even during the transfer phase of the system. These cause the vertical state sequencer to generate the Acq_request signal to the acquistion memory that will correspond to each of the selected vertical input signals. Using the Acq_Request line, the Acquistion memory system will take the current 10 bit A/D value from the acquistion board, via the Input Data Latch, and place it into the Acquistion memory and, then, advance the memory address counters for the next sample. Along with the ten bit A/D value that was stored into the acquistion memory, there are two groups of 3 bits. One of these 3 bit groups identifies which time base the Acq_request was generated by: Main, Window1, and/or Window2. This information is used, later, in keeping track of the number of main and window record points that have occurred. The other group of 3 bits is used to identify the vertical input that produced this A/D sample (this data comes from the Initial ID table). This is driven by inputs from the Vertical State Sequencer and the Plugin Chop Sequencer. The Initial ID table allows us to encode a large number of possible vertical input combinations down into the eight possible vertical sources.

The main trigger is held off by the PRETC signal so that the trigger cannot occur until enough data points have been acquired. The value in the pretrigger counter is determined by finding the maximum number of pretrigger points needed by the main and window records. The output of the pretrigger counter is fed into a section of hardware called the Randomizer. Its function is make the total cycle time of the system more random. If the system is not random in nature, then certain frequencies of input signals will cause the system to not acquire complete records during equivalent time operation. Once the randomizer inserts a random delay into the PRETC path and the PRETC signal arrives on the acquistion board, the acquistion system may now accept the next valid trigger condition. In order for the trigger to be valid, it must also satisfy the holdoff conditions that have been set up. When the first valid trigger occurs, the acquistion board will pass the main trigger signal over to the time base board. At the same time, the window holdoff counter is started (if it is set up) to holdoff the window trigger system, which is constrained to allow only window triggers after the main trigger has occurred. Also, the main time interpolater is now used to measure the amount of time between the trigger occurrence and the next 50 ns clock, which is the basic clock rate of the time base system. This value is sent to the DAG (Destination Address Generator), which uses this number, along with other measured and constant values, to produce the addresses for the data points acquired during this sweep. These addresses are used to position the data points during the transition phase in the waveform memory, which is located on the MMU board in the EXP section of the 11401/11402 system. Once the main trigger signal arrives on the time base board, it will start the main postrecord counter, which is used to count the number of main record points to acquire after the trigger. Each of these points is handled in exactly the same manner as the pretrigger points. The data points in acquistion memory do not carry any time-

keeping information with them, other than their relative position to other points in the same record. Therefore, it can be seen that the flow of these points into acquistion memory must be continuous during the acquisition of the signal, otherwise, the relative time between the points would be altered (this concept will be important during the discussion of the plugin chop system). Once the main post record counter has counted down, thereby filling up the post trigger section of the main record, it will assert its terminal count signal, which will cause several things to happen. First, the flow of rate pulses from the main time base counter will be shut off so that no more main record points will be acquired. Also, it will send a signal to the End Detect Logic that uses this signal, and others like it from the window time bases, to determine the end of the acqusition phase of the cycle.

Now we must dicuss the operation of the window time bases. First of all, while the window time base system supports two fairly independent windows, they share enough hardware and other things to make them appear, at times, as one time base and, at other times, as two time bases. The windows are required to use the same trigger source and to operate at the same rate and duration. But, there are no restrictions upon the position of one window verses the other. The descriptions of window1 and window2 are interchangeable. The 1 and 2 designators are for convenience only. The window time base hardware operates in much the same manner as that of the main time base, although, there are more counters and more modes of operation. There are three types of operation modes for the window time base, they are *runs before windows, pretrigger windows,* and *runs after windows*. All of these modes share elements of the next mode. In other words, the *runs before* mode behaves very similarly to the pretrigger mode. The *runs after* mode uses some common elements of the *pretrigger* mode.

The *pretrigger* mode in the window time base is the most similar mode to that of the main time base's mode of operation. In the *pretrigger* mode, some points are acquired before the window trigger and the remainder of the points are acquired using the individual window post record counter. Since there is only one pretrigger counter in the system, both the main and window time bases must work off of the same counter. As stated previously, the window trigger is common between the two window records, but it may be the main trigger is fed over into the window hardware or it may be a completely separate trigger signal. That, by defintion, must occur after the main trigger has occurred and the window holdoff has timed out.

The *runs after* mode for the windows occurs when the user specifies that the desired position of the window record is some time after the occurence of the window trigger, such that, some time must pass before the window may start acquiring data. In this case, a counter, called the window position counter, is used. Each window time base has one of these, just as each of the windows has their own postrecord counter. This position counter is used to count the number of window rate pulses from the window rate counter, after the window trigger. Once this position counter has counted down, the window's post record counter is started, which causes the window rate requests to be sent off to the vertical state sequencer and handled in a similar manner to that of the main. When this postrecord counter finishes, it will shut off the window time base requests for that window and inform the end detect logic that the window has completed.

The *runs before* case is very different from this situation, as, in this case, the entire window record has been postioned ahead of the window trigger. In order to be able to acquire only the desired points, we would have to know when the trigger was going to occur, since all actions enabling and disabling the acquistion of the window points would have to occur before the actual trigger, even though these points are supposed to be related to the trigger. It turns out that the only simple way to solve this problem is to allow a sufficently long pretrigger time to acquire the entire window record and to acquire all window points that are available until the actual trigger shows up. At that time, the acquistion of the window record's points are

disabled and the end detect logic is signaled to indicate the end of the that particular window record. It should be noted that the 2 window records do not have to be in the same modes, as the modes are set independently for the two window records. In the *runs before* case, the window post record counter is used, not during the acquistion, but during the transfer phase of the cycle, to count back as the DAG is reading points out of the acquistion memory, the number of the particular window record points that it has encountered. Thus, it provides a way to count back in time in order to look at the data that was acquired before the trigger event took place. Once a predetermined number of points have been counted back, the DAG can now treat these window points just as any other type of points.

One other counter that deserves mention is the Trig-to-Trig counter. This counter is used to measure the number of 50 ns intervals between the main and window triggers. Since the main and window time interpolator measure the interval between the trigger and the next 50 ns clock, this information, which is collected by the DAG shortly after the individual trigger events, can be used with the value of the trig-to-trig counter, which must be read via the microprocessor, to achieve trigger to trigger single shot measurements with a resolution of 10 pS and an accuracy of 100 pS.

Once all of the enabled time bases have reported their status as done (the disabled time bases are always treated as finished), the end detect logic makes sure that the vertical state sequencer has completed its last operation and, when appropriate, that the plugin chop sequencer has completed its work (if it is in a special mode called 'Single Shot Chop'). More about the plugin chop sequencer and its modes later on. Once all of these checks have been performed, the end detect logic will provide a signal, called Acq/Xfer, to the DAG and to the Acquistion memory system. This signal is used to switch modes in both places. For the DAG, it tells it to start trying to read the acquistion memory. To the acquistion, this signal, Acq/Xfer, switches the mode from "write" to "read" and changes the direction of the automatic address counters. Neither the time bases nor the DAG need to know the absolute address of a piece of data, only the relative position to the next sample from the time base. Because the acquistion memory uses a post-increment and post-decrement mode of operation, the hardware performs a dummy read cycle at this time to correctly position the address counters to the lastly acquired piece of data, rather than, to the next available location in acquistion memory. The acquistion memory consists of 4 banks of 4K by 16 bit words for a total of 16k words.

Once the acquistion memory has turned around, the DAG starts to request waveform points via the Dag_Request line. It should be noted that the DAG always starts at the end of the record and works to the start of the record. For each point, the DAG will request a point from the memory, this point may contain a point for the main, window1, and/or window2 records. The DAG never sees the data contained in the waveform point, but looks directly at one of the 3 bit groups and, indirectly, at the other 3 bit group. As noted above, one of the 3 bit groups, called the horizontal tags, is sent to the DAG so that the DAG can keep track of the relative positions of each of the records. The DAG will look at the first of the waveform tags and check to see if the data point is for that particular record, if not, it will move on to the next tag bit. Otherwise, it will make the necessary calculations for that point and either generate an address for it, or discard it (for a variety of reasons). A point can be disgarded: if, it is part of the system overrun (more about this later); if, the record, which has to be a window, is in *runs before* and this point is before the record; and if, the point follows a record that has already been completely sent or it has been marked Invalid by the final ID table. Under most circumstances, even though a point is disgarded, the DAG actually uses this information to update internal and external counters in order to keep track of the current position.

The other group of tag bits is used to encode the vertical source of that sample data. This set of three bits is applied to the Final ID table, along with two bits from the DAG that indicate

request will cause a word to read from memory and to be written into the interface port. In the process of writing data to the interface port the DMA request line is cleared. Once the device on the other end of the interface has acknowledged the transfer, the DMA request will be reasserted.

CPU & Ready Logic (diagram 33)

The Display Controller board's incoming and outgoing data is serviced by U524's programmable DMA (Direct Memory Access) unit. The DMA provides the following two independent channels. The DRQ0 (pin 18, Data Request line) that serves the incoming data channel, and DRQ1 (pin 19, Data Request line) that serves the outgoing data channel.

You should note that transfers from the interface port into memory is a source-synchronized transfer, while the transfer from memory to the interface is a destination-synchronized transfer. The interface port has been designed to run without any waitstates. That is, it's a zero waitstate device. Microprocessor U524 uses PCS4 to access this port, so currently this port is selected between 0200*hex* - 027F*hex* in the I/O space.

Waveform Attribute Encoder (diagram 37)

This circuit facilitates high-speed transfers of incoming information. The digitizer and waveform processing systems in this instrument dictate that the waveform data format is a left justified 10-bit word. This 10-bit word is transmitted in a 16-bit word, with the lower 6-bits being considered as "don't cares", with three exceptions. These three exceptions are Null, Overrange, and Underrange, and their values are passed as 8000*hex*, 7FFF*hex*, and 8001*hex*, respectively. The Waveform Attribute Encoder stage uses PAL (Programmable Array Logic) to decode these special cases and set the appropriate bits in the trace data word. The Null bit in the display word may be set on any data passing through the Waveform Attribute Encoder, regardless of the value of the data. This "Null force" condition is enabled by asserting bit 4 of port 1 of U523 (pin 35) on diagram 33.

The waveform data that is sent to the Display Controller board from the Compressor board is in a 2's complement format. In order to support the VRS (Vertical Raster Scan) system, which requires 9-bit data ranging between 0 and 1FF*hex* inclusive, the data must be transformed and shifted. The number format transformation is accomplished by inverting the most significant bit of the incoming data. The shifting of the incoming trace data is further complicated because the VRS system can support two display modes; the single and the dual axis modes. When the VRS system is operating in the single-axis mode the incoming data is shifted to the right by 6-bits. When the display is operating in the dual-axis mode the data must be shifted to the right by 7-bits. This will adjust for half the dynamic range of the individual axes. A bit coming from the MUART (Multifunction Universal Asynchronous Receiver Transmitter) circuit, port 1, bit 7 (U523, pin 32 on diagram 33) is used to supply an offset to the encoded trace data word. When this bit (offset) is cleared, the waveform will be displayed in the lower half of the display, because the resultant data values range between 0 and OFF*hex*. When the offset bit is set, the waveform will be displayed in the upper half of the VRS display area, since the resultant data is within the range of 100*hex* to 1FF*hex*.

ROM & Select (diagram 33)

EPROM's U602 and U612 comprise the standard firmware for the Display Controller board, with U602 being the high order byte. The standard firmware EPROM's may be configured for use by three different types of EPROM's, depending upon the amount of storage needed. Refer to Table 1 for further information.

Table 1
Standard Firmware EPROM's Storage Capabilities & Jumper Settings

EPROM Type	Jumper Setting J7	Size In J12	Address Bytes	Range (In *Hex.*)
27128	128	256	32K	F8000 - FFFFF
27256	256	256	64K	F0000 - FFFFF
27512	256	512	128K	E0000 - FFFFF

EPROM's U700 and U712 comprise the optional firmware for the Display Controller board, with U700 being the high order byte. The optional firmware EPROM's may be configured for use by three different types of EPROM's, depending upon the amount of storage needed. Refer to Table 2 for further information.

Table 2
Optional Firmware EPROM's Storage Capabilities & Jumper Settings

EPROM Type	Jumper Setting J8	Size In J13	Address Bytes	Range (In *Hex.*)
27128	128	256	32K	D8000 - DFFFF
27256	256	256	64K	D0000 - DFFFF
27512	256	512	128K	C0000 - DFFFF

The EPROM's are selected via the ROMCS(L) line on processor U524, pin 34. When U524 is reset, the ROMCS(L) line is the only Chip Select Unit line that is active, and only then for the address range of FFC00*hex* - FFFFF*hex* (the upper 1K of memory). The ROMCS(L) line also sets up a 3 waitstate delay in every EPROM access, and it looks at the external ready line.

Microprocessor Data Latch (diagram 33)

The Microprocessor Data Latch stage is comprised of data bus drivers U615, U621, gate U427C, and inverter U634F. Address and data information is multiplexed together onto a common set of pins (U523, pins 1 through 8). This necessitates locating the MUART and the microprocessor on the same local bus (before the Microprocessor Data Latch stage). When the microprocessor supplied signals DT/R(L) and DEN(L) are used to control latches U615 and U621, the data bus will actually be demultiplexed, in that the address does not appear on the data bus. Since the address does not appear on the data bus, the MUART chip is the only component other than the bus drivers to reside on the local microprocessor bus, lines PD0 - PD15. In order to prevent contention with the Microprocessor Data Latch stage during a MUART access, the DEN(L) signal is gated with the MUARTCS(L) line, which is the PCS(L) on the microprocessor. With this gating the Microprocessor Data Latch stage is disabled during any request to the MUART.

The MUART is accessed via the microprocessor Control Bus using the MUARTCS(L) line, which is connected to the PCS0 line, pin 25 on the microprocessor. All requests to this line requires that three wait states be inserted.

The Display Controller Board's microprocessor, U524, can be run in a Forced Instruction Mode. This allows a person to observe the address lines in operation, and to detect a faulty component, using signature analysis. This is the only place where diagnostics software is not used, as the address lines are assumed faulty at this point, and the software cannot run.

The Display Controller Board circuitry will operate in the Forced Instruction Mode when jumpers J5, J6, and J11 are moved from the Norm position, to the Test position. This forces data bus drivers, U615 and U621, into the disabled mode. Jumpers J5 and J11 cause the two microprocessor local data bus lines, PD1 and PD9, to be pulled down to ground. This, in turn, will cause microprocessor, U524, to receive a FDFD*hex* instruction code, which is a STD instruction. Since this is in effect an NOP instruction, the microprocessor will continue to fetch this instruction and progress through the address range. A note should be made that microprocessor U524 will not sequentially go through memory, as the CS register is set to FFFF*hex* upon power up. With IP register being set to zero, this will cause the address sequence to be FFFF0*hex* → FFFFF*hex*, then OOOOO → OFFEFF*hex*, then back to FFFF0*hex*. Further, the chip select line for the ROMs will be active during the passage through FFFF0*hex* to FFFFF*hex*.

Microprocessor Address Latch (diagram 33)

The Microprocessor Address Latch stage is comprised of address bus drivers U526, U614, and U620. The ALE (address latch enable) signal from U524, pin 61, is active high to latch the addresses into the three bus drivers. The rising edge of the ALE signal is generated off the rising edge of the MPUCLK signal. Addresses are valid on the trailing edge of the ALE signal.

Diagnostic Loopback Control (diagram 37)

The Diagnostic Loopback Control stage is comprised of U623A,B,C,D, U630A,C,D, and U634A. When the LOOPBACKEN(L) bit is set, it causes this stage to make the Executive Processor Parallel Interface Port stage look busy. This strobes handshake lines, SENDNEW(L) and DATARDY(L), to transfer data from one side of latching ports U731 and U733, to the other. The transfer occurs when microprocessor U524's Chip Select strobes the BMLCS(L) line, by reading from I/O address 280*hex*.

General Purpose Static RAM (diagram 33)

The General Purpose Static RAM (hereafter called GPSRAM) is comprised mainly of RAMs U601 and U611. The start of the RAM address space serves as an interrupt table for microprocessor U524.

The Display Controller will be provided with 4K of RAM when Jumper J9 is installed in the 4K position and both 6116P RAMs (U601 and U611) are installed at the bottom of their sockets leaving pins 1, 2, 27, and 28 open. If it becomes necessary to provide more GPSRAM space, an

alternate set of 6264P RAMs may be used. When 6264P RAMs are installed in the Display Controller, jumper J9 must be moved to the 16K position.

Interface Data Buffers (diagram 37)

The Interface Data Buffers stage is comprised of octal bus transceivers U713, U720, and gate U721D. This stage provides synchronous two-way communications between the interface port and the microprocessor data bus.

Waveform Data Buffers (diagram 37)

The Waveform Data Buffers stage is comprised of octal buffer/drivers U616, U622, gates U721A,B, and inverter U636F.

MUART (diagram 33)

The **MUART (Multi-function Universal Asynchronous Receiver Transmitter)** stage is comprised of interface IC U523. It provides 16 lines of parallel I/O, a serial port, a baud rate generator, various timers, and an interrupt controller. The display controller uses the parallel I/O to provide software control of various portions of the display hardware. The serial port is used to provide a diagnostic communication path between the waveform processor (on the A16 Compressor Board) and the display controller. MUART U523 is also used to develop software for the display controller, and to provide interrupts to microprocessor U524 in the CPU & Ready Logic stage.

Because of the limited number of pins available on the U523 MUART chip, the address and data information is multiplexed together onto a common set of pins (pins 1 through 8). This necessitates locating the MUART and the microprocessor on the same local bus (before the Microprocessor Data Latch stage). When the microprocessor supplied signals DT/R(L) and DEN(L) are used to control the Microprocessor Data Latches U615 and U621, the data bus will actually be demultiplexed, in that the address does not appear on the data bus. Since the address does not appear on the data bus, the MUART chip is the only component other than the bus drivers to reside on the local microprocessor bus, lines PD0 - PD15. In order to prevent contention with the Microprocessor Data Latch stage during a MUART access, the DEN(L) signal is gated with the MUARTCS(L) line, which is the PCS(L) on the microprocessor. With this gating the Microprocessor Data Latch stage is disabled during any request to the MUART.

Serial port lines TxData(L), RxData(L), and COMCLK are connected to to interface connector J52. Only the TxData(L) is an output. These are 5-volt only signals, and while the format is compatible with RS-232-C interface, a voltage converter must be set up before an RS-232-C device may be connected to the serial port. The MUART only supports one handshake line which has has been hard wired to the active state.

The MUART is accessed via the microprocessor Control Bus using the MUARTCS(L) line, which is connected to the PCS0 line, pin 25 on the microprocessor. All requests to this line requires that three wait states be inserted.

Video Shifter Control (diagram 34)

The Video Shifter Control stage is comprised of gates U630B, U432A, and positive edge-triggered flip-flop U425B. The BSRLOAD (Bit-plane Shift Register Load) signal is generated by the detection of the video hardware phase of the video memory. That is, when CCLK, FCLK, LCLK, and MCLK are all high, and U630B is gated by the Display Enable signal from the CRT Controller & Select stage (pin 18, U515). The presence of the Display Enable signal at pin 18 of U515 indicates a valid CRT Controller & Select stage video memory address. This detection signal is clocked by the rising edge of the PCLK signal into pin 11 of U425B. This allows the signal on pin 6 of U432A to be sampled on the falling edge of PCLK by the Plane 1 and Plane 2 Video Shifter stages, U220 and U221, and thereby cause them to latch the data from the Bit Plane 1 and Bit Plane 2 DRAM (video memory) stages.

CRT Controller & Select (diagram 34)

The CRT Controller and Select stage consists mainly of U515 and U534. This stage is the basis for all timing in the video portion of the Display Controller Board. The chip select, CRTCS(L), causes a positive-going pulse to be formed using U534, U525E, and U517D. Latch U631A is used to latch the R/W(L) signal so that it will meet the hold times of controller U515. The data bus lines (MD0-7) run to controller U515 (D7-D0). Using MA1 (U515, pin 24) as a register select signal, the command and data registers are both placed on the same side of the data bus. The CRT Controller & Select stage is selected through the microprocessors PCS1 pin, named CRTCS(L). This chip select must be set up for a three wait state delay for every CRT Controller & Select stage request.

On the video side of the CRT Controller & Select stage, the master video clock is set at 2.0 megahertz, using the CCLK line. This sets the word display time to 500 nanoseconds. CRT Controller U515 generates a new address on every falling edge of its master clock. This new set of addresses is passed on to the Bit Plane Address Mapping stage and to the VRS Plane Address MUX stage. Since the new addresses are not required until the rising edge of CCLK the crt controller has plenty of time to generate the new addresses. The Display Enable signal (U515, pin 18) is handled in much the same way. Display Enable is used to generate a load pulse to the Video Shift Control stage.

The LPEN input (U515, pin 3) is used by the diagnostics hardware to determine where the crt controller thinks it is, with relation to the address values being presented on the Diagnostic Timing MUX stage.

Video Memory Buffer & Select (diagram 33)

Bus driver/latches U502, U503, U512, and U513 mainly comprise the Video Memory Buffer and Select stage. The most important function of this stage is to provide a way for the slower microprocessor to latch data from the high-speed video memory. It also serves to reduce loading on the microprocessor Data Bus. The drivers or latches are enabled depending upon the direction of the data transfer and when VSEL(L) is generated from the Video Memory Interface Synchronizer stage. The 16-bit Video Data bus (VD0-15) is a local bus that is used just for transfers between the video memory and the microprocessor.

Diagnostic CRTC/MPU Address Trigger Control (diagram 5)

The Diagnostic CRTC/MPU Address Trigger Control stage is comprised of U401A,B,C,D, U402A,B, and U517A. The video address registers U500, U501, U510, and U511 capture all 14-bits of the CAS(L) addresses. They also capture the RA0, RA1, RA2, and RA3 lines from U515 in the CRT Controller & Select stage. The registers are triggered in two parts so that the CAS(L) cycles may be captured, by U401, which is driven by the Diagnostic CRTC/MPU Address Trigger Control stage. The trigger signal is also sent to the LPEN (light pen) input of U515 in the CRT Controller & Select stage. Only one trigger signal is generated. Another trigger will not occur until the VRLCS(L) line is pulsed, indicating that all of the previously captured data has been read. The type of trigger (crt address or microprocessor address) is determined by the state of the trigger bit in the 'write only' diagnostics register, U600, pin 16, located at I/O address 101*hex*. The address latches are read only registers.

Diagnostic Bit & VRS Plane Address Feedback Latches (diagram 37)

The Diagnostic Bit & VRS Plane Address Feedback Latches stage is comprised of 8-bit registers U500, U501, U510, and U511. These video address registers capture all 14-bits of the CAS(L) addresses. They also capture the RA0, RA1, RA2, and RA3 lines from U515 in the CRT Controller & Select stage. The registers are triggered in two parts so that the CAS(L) cycles may be captured, by U401, which is driven by the Diagnostic CRTC/MPU Address Trigger Control stage. The trigger signal is also sent to the LPEN (light pen) input of U515 in the CRT Controller & Select stage. Only one trigger signal is generated. Another trigger will not occur until the VRLCS(L) line is pulsed, indicating that all of the previously captured data has been read. The type of trigger (crt address or microprocessor address) is determined by the state of the trigger bit in the 'write only' diagnostics register, U600, pin 16, located at I/O address 101*hex*. The address latches are 'read only' registers.

The microprocessor address trigger will occur upon the first GATE signal generated by U426A, pin 6 of the Video Interface Synchronizer stage, after the VRLCS(L) register bank has been read. The crt controller address trigger will occur at the first CCLK(L) time after Display Enable has gone high, and after the VRLCS(L) register bank has been read.

Diagnostic Timing MUX (diagram 37)

The Diagnostic Timing MUX stage is comprised of multiplexers U433, U530, and flip-flops U516A, U516B. The purpose of this stage is to provide a means of examining a large number of repetitive signals, and to feed a number of them into the Programmable Timers (pins 20 and 21) of the U524 microprocessor. A means is also provided to route a subset of these signals into the Data In (pin 34) of the MUART, U523. In addition to handling the signals that are too fast for the microprocessor, a subset of these signals are passed through a divide by 4 circuit to reduce their rate. The multiplexers, U433 and U530, are used to multiplex the various signals in the Display Controller Board circuitry into two input streams. The two multiplexers have common select lines (pins 1, 2, and 4) that select the source for their outputs. These select lines are driven by a diagnostics write only register located at I/O address 101*hex*. Another line from this register provides a means to reset the divider circuitry and to force its output to the high state. In order to let the microprocessor test the timers internally, the timer input pins must be held at a high level.

The output of the low-speed signal multiplexer is also connected to the DATA IN input to MUART U523. When the proper input selection is made, the DOUT (diagnostics output) pin 59 of gate array U125 can be routed to the MUART input. This also provides a way for the software to directly find the current state of the sync signals for the timing of various display events.

System Timing Generator (diagram 34)

The System Timing Generator stage is comprised mainly of oscillator Y430, divider U431, U435A, and an associated chain of gates. This stage generates all timing signals for the Display Controller Board. Refer to Figure AA, Display controller system timing diagram.

Figure AA. Display Controller System Timing Diagram

These timing signals are derived from a 32 megahertz clock that is generated by oscillator Y430, and with one exception, do not depend upon gate delays to produce the correct signal. The 32 megahertz oscillator provides the required crt pixel rate, and is divided down to produce 16 megahertz, which is the highest possible microprocessor clock rate.

In order to provide the automatic board test system with access to the timing chain, U332D and U532D were added to the basic circuit. They provide the means of halting the 32 megahertz clock and of supplying a new clock signal to the System Timing Generator circuitry. When pin 12 of U332D (connected to pull-up resistor R534) is brought low with a test probe, the oscillator signal will be blocked from the remainder of the System Timing Generator's circuitry. The pulled-up input of U532D, pin 12, may now be toggled externally to provide a new clock signal.

The output of gate U532D, pin 11, is connected to the input of clock divider U431, pin 2, and to the input of U427B which is the only gate delay element on the Display Controller Board. Gate U427B delays the 32 megahertz clock signal sufficiently that the signal edges occur near the times when the outputs of divider U431 changes states. The output of U427B is inverted by U434B to provide the PCLK (pixel clock) signal to the Display Controller Board circuitry. This signal is again inverted by U434C to provide the PCLC(L) signal. This signal is used only in the DRAM Control Generator stage. The slight delay of the PCLK(L) signal caused by U434C gives the DRAM Control Generator stage more time to set up the inputs for the various elements.

The 32 megahertz signal is divided into four sub multiples by U431. These are MCLK (microprocessor clock) at 16 megahertz, LCLK at 8 megahertz, FCLK at 4 megahertz, and CCLK (character clock) at 2 megahertz. An inverted version of CCLK is generated by U434E. The CCLK signal is also used by U435A to generate LCCLK(L) (Late CCLK). The LCCLK(L) signal is used to provide a window in which the DRAM accesses may occur. A single DRAM operation may occur in either or both half cycles of the LCCLK(L) signal. This delayed signal allows the video hardware to latch the data at the very end of their memory cycle, while the DRAM's are still holding valid data at their outputs. This delayed clocking scheme also allows the Video Memory Interface Synchronizer stage time to resolve the marginally stable conditions within some of its flip-flops. The LCCLK(L) signal is also used as the video phase RASE (Row Address Strobe Enable) signal, which is the counterpart of the Gate(L) signal for the microprocessor phase of the video memory cycle.

The MCLK (Microprocessor Clock) signal is used to drive microprocessor U524. The microprocessor produces a lower-frequency clock (8 megahertz) from this signal which is used as

its bus clock. This 8 megahertz clock signal must not be interchanged with the LCLK 8 megahertz signal.

DRAM Control Generator (diagram 34)

The DRAM Control Generator stage, as its name implies, generates the basic timing signals to operate the Dynamic Random Access Memory systems on the Display Controller Board. The control signals used for the VRS Plane DRAMs are the same as those used for the Bit Plane DRAMs. The timing relationships for these control signals are shown in Figure AB.

Figure AB. DRAM Control Generator Timing Diagram

In addition, this stage also generates a few signals that are used in various other places on the Display Controller Board. Shift register U326 is the heart of this stage, and its output looks like a delay line with 31.25 nanosecond steps (refer to the timing diagram in Figure AA).

Together, U427A and U434A generate a combination of signals that is input to U425A to form a single pulse at the start of each memory cycle. This pulse is injected into shift register U326, pins 1 and 2. Shift register U326 is simultaneously being clocked by the PCLK(L) signal to form a 'solid-state delay line.' This delay line will produce a single pulse on each of its 8 output lines (Q0 through Q7) during each memory cycle. These pulses are used to control the state of the RS flip-flops that are constructed from NAND gates (U332A,B, U333A,B,C,D). The output of these RS flip-flops are the DRAM control signals. The output of the solid-state delay line is also used to generate VDLATCH (pin 10 of U732C), which is used to latch data from a microprocessor read, from the video memory. A few of the outputs of the delay line are used directly for other control lines. Q3 is used in the Video Memory Interface Synchronizer stage. Output Q6 is used by the diagnostics hardware to latch the RAS addresses from the DRAM address multiplexers. Output Q7 is used to latch the word select lines VA1 and VA1(L) sufficiently early enough to set up the DRAM control circuitry.

Diagnostic Control/Status Latch (diagram 37)

The Diagnostic Control/Status Latch is comprised of registers U600, U610, gates U613D,C, and LEDs DS500, DS501. In some cases the Display Controller Board circuitry may not be able to indicate a malfunction. To solve this problem, two LEDs (DS500 and DS501) have been provided to give a visual indication of the current diagnostic test status. In addition to the two LEDs, the output of U610 is connected to eight square pins (Diagnostic Status Pins, 0 through 7). The state of these LEDs and square pins is determined through software. The LEDs are controlled using two bits from the diagnostics write only register, located at I/O address 101*hex*. This register, U600, is reset to all zeros when the X RESET (external reset) line on the parallel interface is driven low. The state of the Diagnostic Status Pins (0-7) is set by the value written into the write only register U610, located at I/O address 100*hex*. This register is reset to all zeros when the X RESET line is driven low.

Video Memory Interface Synchronizer (diagram 34)

The Video Memory Interface Synchronizer stage is the heart of the interface between the microprocessor and the display memory. This stage is responsible first to recognize a request for access to the display memory, then to hold off the microprocessor while a request signal is generated and acknowledged by the video memory, and finally to release the microprocessor.

The operation of this stage begins when a midrange chip select (MCS0-3) is generated by the microprocessor. The chip selects become valid sometime after the beginning of T1 of the microprocessor. The signal is latched at the falling edge of clock MPUCLK (start of T2).This stage of delay is necessary because the microprocessor generates it's chip selects before the RD(L) and WR(L) strobes become valid. At the halfway point of T2 the request is passed to the next stage. This stage generates the SRDY(L) (Synchronous Ready) signal to the microprocessor. This signal will easily be setup in time to meet the setup times for the microprocessors SRDY line. At this point the request is passed to the video memory side of the interface.

The request from the microprocessor side of the Video Memory Interface Synchronizer stage is now present at the input of the video memory side of the interface, waiting to be accepted. At the next falling edge of the CCLK signal, the request is passed to the next stage, which is a slightly delayed version of CCLK. This delay allows two things to happen. First, any metastable condition induced by the transferring of the microprocessor request to the asynchronous video interface, will have had time to settle out. Second, this delay allows the memory cycle to have data present and valid at the very end of the video hardware display cycle when the video data is latched. Once the request is clocked through the LCCLK flip-flop, it becomes knows as GATE. The GATE signal will only go low during the MPU portion of the video memory access time, and it will appear only once during any single microprocessor request. The GATE signal is used to re-decode the chip select into a plane request. This plane request will enable the hardware of the desired plane into generating a microprocessor memory request.

As the microprocessor memory cycle proceeds, the Q3 timing signal into pin 12, U337D in conjunction with the GATE signal into pin 6, U426A, will reset the microprocessor request. This will clock a flip-flop to assure that this signal is present during the next MPUCLK rising edge. Once this rising edge occurs, the request will be removed from the input of the video memory side of the Video Memory Interface Synchronizer stage. Also, the SRDY (Synchronous Ready) signal will be removed from the microprocessor, thereby allowing the microprocessor to continue the memory cycle. The Q3 signal is timed such that the video memory request will be removed from the video side before the start of the next MPU portion of the video access window. Also, if the operation requested was a read, the reset signal to the microprocessor side of the Synchronizer stage must occur late enough for the video memory cycle to complete and latch the data into the bus interface unit. The read data is latched into the bus interface unit by a combination of timing signal Q7 and GATE.

Once the microprocessor begins to finish the memory cycle, it will remove the chip select. When the chip select signal goes high it will reset the flip-flops in the microprocessor side of the Synchronizer stage. This action will prevent the Synchronizer stage from locking out another immediately following video memory request. When a string operation is being done in the video memory, the microprocessor only holds the chip selects high for just a few tens of nanoseconds before the next cycle is begun.

Bit Plane Address Mapper (diagram 34)

The Bit Plane Address Mapper stage consists of 4-bit binary full adders U412, U424, U428, U514, U520, and U521. This stage is used to reduce the memory requirements of the two Bit Plane DRAM stages. The CRT Controller & Select stage is programmed such that considerable memory between scan lines is unused if linear mapping is done between the addresses that are output by the CRT Controller & Select stage and the two Bit plane DRAM stages. The Bit Plane Address Mapper stage allows this unused memory space to be compressed to a much smaller value.

This stage condenses the offset between adjacent scan lines from 64 words down to 48 words. In the row/column mode of the CRT Controller & Select stage, the row addresses are incremented by "one" every time the column addresses progress through an entire count sequence. The column count sequence is actually between only 0 and 43. The other addresses generated at the end of the scan line (during raster retrace) are not needed, so they are ignored. From word 0 in one scan line to word 0 in the following scan line the addresses will advance by 48 (or 30*hex*). If the row address is considered as the scan line count, it could be multiplied by 30*hex* to get the proper offset for each scan line. Because 30*hex* is not a simple shift, the column address is added back into the newly converted row address to create the new address bit. This is accomplished by the first three 4-bit adders U514, U520, and U521. A multiplication by 10*hex* is performed by just offsetting the bits that get added to the column addresses, therefore, the lower 4 column address bits are passed undisturbed. Then, the final three 4-bit adders U412, U424, and U428 are used to add the new version of the row address to the proper bits of the column address. This stage will complete the above operation in between the time that the CRT Controller & Select stage generates the new addresses and the occurrence of the rising edge of the CCLK signal, which is when the new addresses are used.

Bit Plane Address MUX (diagram 34)

The Bit Plane Address MUX (Multiplexer) stage is comprised of U404. U410, U414, U421, U403, U400, U634E and U325B. This stage is used to multiplex the crt addresses for the bit planes and the microprocessor's addresses. Within this stage there are two sets of multiplexers. The first set performs the actual address multiplexing, and the second set multiplexes the results of the first set. The output of this stage provides the multiplexed addresses required by the Bit Plane 1 and 2 DRAM (Dynamic Random Access Memory) stages.

This stage performs a fairly simple transformation, as the least significant bit of the Bit Plane Address Mapper stage output is paired up with the least significant "word" address bit from the microprocessor. These multiplexers are controlled by a buffered and slightly late version of CCLK, with the exception of the least significant multiplexer. The low order multiplexer uses an unbuffered version of CCLK and a faster chip to ensure the VA1 line sets up flip-flop U325B soon enough. These multiplexers are controlled by the COLADR (Column Address) signal from the DRAM Control Generator.

VRS Plane Address MUX (diagram 34)

The VRS Plane Address MUX (Multiplexer) stage is comprised of U405. U411, U415, U423, U413, and U420. This stage is used to multiplex the crt addresses for the VRS Max Plane DRAM and VRS Min Plane DRAM stages, and for the microprocessor's addresses. Within this stage there are two sets of multiplexers. The first set performs the actual address multiplexing, and

the second set multiplexes the results of the first set. The output of this stage provides the multiplexed addresses required by the VRS Max and Min Plane DRAM (Dynamic Random Access Memory) stages.

The input selection for the multiplexers is done using the same buffered CCLK signal that the Bit Plane Address MUX stage uses. This stage performs the same function for the VRS (Vertical Raster Scan) as the Bit Plane Address MUX stage performs for the two Bit Plane DRAM stages. That is, to put the most rapidly changing address bits in the row address lines. These multiplexers are controlled by same signal (COLADR line) as the Bit Plane Address MUX.

Bit Plane 1 & 2 DRAM Control (diagram 35)

The following discussion will cover both the Bit Plane 1 DRAM Control and the Bit Plane 2 DRAM Control as one stage. The bit plane memory system is constructed of 64K Dynamic RAMs in a 16K X 4 configuration, running at a cycle time of 250 nanoseconds. The bit planes respond to memory requests from two sources.

First, from the video hardware, which needs refreshing every 500 nanoseconds. This request is formed by using the high state of the ACCLK signal, which is an inverted version of LCCLK(L) (Late Character Clock).

Second, from the combinations of the GATE(L) signal, and from the midrange chip select lines from microprocessor U524. The video hardware requests are always word reads, while the microprocessor requests can be read or write, either byte or word type.

Once the request has been formed it is used along with a buffered version of CAS(L), and a word select line, VA1 and VA2(L), in order to determine which set of chips to send the request. The RAS signal is combined with the RASE signal to produce a signal (Q6 of U326) to the RAMs that will only occur when there is a valid cycle to be performed. Because the least significant bit is lost due to the word select line, twice as many addresses must be presented to the DRAMs in order to keep them refreshed.

When a microprocessor request occurs, the RAS signal is also sent to the other plane. The WE(L) signal (pin 8 of U320C) is constructed using the R/W(L) signal from the microprocessor and combining it with the GATE signal, so that a WE(L) can only be created during a microprocessor memory cycle.

Bit Plane 1 DRAM (diagram 35)

The Bit Plane 1 DRAM stage is comprised of dynamic random access memories U210, U211, U212, U213, U214, U215, U216, and U217. The following discussion will cover both the Bit Plane 1 DRAM and the Bit Plane 2 DRAM stages, since implementation of the two planes are identical, except where noted. The memory system is constructed of 64K Dynamic RAMs in a 16K X 4 configuration, running at a cycle time of 250 nanoseconds. The bit planes respond to memory requests from two sources.

First, from the video hardware, which needs refreshing every 500 nanoseconds. This request is formed by using the high state of the ACCLK signal, which is an inverted version of LCCLK(L) (Late Character Clock).

Second, from the combinations of the GATE(L) signal, and from the midrange chip select lines from microprocessor U524. The video hardware requests are always word reads, while the microprocessor requests can be read or write, either byte or word type.

Once the request has been formed it is used along with a buffered version of CAS(L), and a word select line, VA1 and VA2(L), in order to determine which set of chips to send the request. The RAS signal is combined with the RASE signal to produce a RAS(L) signal to the RAMs that will only occur when there is a valid cycle to be performed. Because the least significant bit is lost due to the word select line, twice as many addresses must be presented to the DRAMs in order to keep them refreshed.

When a microprocessor request occurs, the RAS signal is also sent to the other plane. The WE(L) signal (pin 8 of U320C) is constructed using the R/W(L) signal from the microprocessor and combining it with the GATE signal, so that a WE(L) can only be created during a microprocessor memory cycle.

Bit Plane 2 DRAM (diagram 35)

The Bit Plane 2 DRAM stage is comprised of dynamic random access memories U310, U311, U312, U313, U314, U315, U316, and U317. Since the function of this stage is identical to that of the Bit Plane 2 DRAM stage described previously, you must refer to that stageheading for a circuit description.

Plane 1 Data Buffer (diagram 35)

The Plane 1 Data Buffer stage is comprised of octal bus transceivers U200 and U201. This stage provides synchronous two-way communications between the bit 1 data bus and the video data bus.

Plane 2 Data Buffer (diagram 35)

The Plane 2 Data Buffer stage is comprised of octal bus transceivers U300 and U301. This stage provides synchronous two-way communications between the bit 2 data bus and the video data bus.

Plane 1 Video Shifter (diagram 35)

The Plane 1 Video Shifter is comprised of register U220. Bit data that is read from the Bit Plane 1 DRAM stage is latched into the video shift register U220, then shifted out serially. The shifted data is passed to the VRS Generation & Control stages custom gate array, U125, for further processing.

The bit map data is presented to the input of the 16-bit video shift register, U220, at the end of the video hardware memory cycle. This data is latched into the video shift register upon the falling edge of the PCLK signal, when the BSRLOAD signal is held high. The least significant bit of the video memory word is shifted out first. This shifted data is fed into flip-flop U230A,B, whose active high drives the CNTE (counter enable) on gate array U125.

For the current monochrome implementation of the Display Controller Board circuitry, there are only two planes of video memory; the Bit Plane 1 DRAM, and Bit Plane 2 DRAM stages. Their video shifter outputs, BP1 and BP2, respectively, are fed into the corresponding inputs of the VRS Generation & Control stage, U125. The BP0 input, pin 55, of U125 is connected to ground for this implementation. If another plane was to be added, its video shifter output would be connected to the BP0 input.

Plane 2 Video Shifter (diagram 35)

The Plane 2 Video Shifter stage is comprised of register U221. Since the operation of this stage is essentially the same as that of the Plane 1 Video Shifter stage above, only that stage will be described.Refer to the Plane 1 Video Shifter stage heading.

VRS Plane DRAM Control (diagram 36)

The Video Raster Scan Plane Dynamic RAM Control stage is comprised of U222B, U223A,B,C,D, U330A,B,C,D, U334C,D,E,F, U335B,C, U336B,C, and associated components.

VRS Max Plane DRAM (diagram 36)

The VRS (Video Raster Scan) Max Plane DRAM stage is comprised of Dynamic Random Access Memory devices U120, U121, U122, and U123. The following discussion will cover both the VRS Max Plane DRAM and the VRS Min Plane DRAM stages, since they operate the same. Further, in most respects these two stages are the same as the Bit Plane 1 and Bit Plane 2 DRAM stages. The major difference between these two pairs of stages is, while the bit planes each produce a 16-bit word on each video hardware memory cycle, the VRS planes memory each produces a 32-bit word. In order to interface with the 16-bit microprocessor bus, The 64K byte VRS memory plane has been divided into two 32K byte planes. Even though the VRS memory system requires about 9 display cycles at the start of each scan line, the RAM will generate data on every video hardware memory cycle. This eliminates the necessity of more logic to decode the valid times for the VRS.

The word select lines are used only to decode the microprocessors request into the proper bank, as opposed to the bit planes where the word select lines were used to select between banks for all memory requests. Like the bit plane memory, the VRS memory is both byte and word addressable from the microprocessor. The same WE(L) signal is used for this memory.

VRS Min Plane DRAM (diagram 36)

The VRS Min Plane DRAM stage is comprised of Dynamic Random Access Memory devices U110, U111, U112, and U113. Since the operation of this stage is similar to that of the VRS Plane Max DRAM stage described previously, you must refer to that stage heading for a circuit description.

VRS Plane Data Buffers (diagram 36)

The Vertical Raster Scan, Plane Data Buffers stage is comprised of octal bus transceivers U100, U101, U102, U103. This stage provides combined synchronous two-way communications between the Video 0 Data/Video 1 Data busses and the 16-bit Video Data output bus.

VRS Generation & Control (diagram 36)

The VRS Generation and Control stage is comprised of custom gate array U125, and associated components U124, U224A,B,C, U230A,B, U231, and U337A,B,C. Gate array U125 has a gate density of about 3000 gates. This gate array provides the Display Controller Board circuitry with a high-speed method of translating waveform data from the waveform processor circuitry into a displayable image. To this end the U125 gate array is placed between the output of the bit planes and the input to the CRT Driver Board circuitry. The U125 gate array is capable of handling a color display system. The VRS (Vertical Raster Scan) system requires nine 29-bit display words to be loaded into the gate array before the VRS display time of each scan line. In the current implementation, there are 160 pixels presented on the current scan line before the VRS system is enabled. The U125 gate array combines the bit plane's video data with the data that it generates to produce the final video output.

The U125 gate array contains a color lookup table and some diagnostics support hardware. These functions are accessed using serial interfaces that are driven by microprocessor U524.

As stated previously, in the current implementation of the Display Controller Board circuitry, the VRS display time starts 160 pixels after the start of the scan line. Before the start of the VRS time, the internal registers must be loaded and the device's counters must be initialized. The control signals for these operations are generated by PAL (Programmable Array Logic) U231. The register load signals CSR0(L) to CSR7(L) and CSRC(L), (pins 1-8 and 63, respectively) occur at the end of the video hardware memory cycle. These active low signals are actually generated by the 3 to 8 decoder, U124, by the Enable signal (U231, pin 19), and the low order address lines of the crt controller. The current implementation makes use of the fact that the low order address lines always progress through the 0-F sequence at the beginning of each scan line, undisturbed by the actions of the mapping hardware, and independent of the actual scan line that is being displayed. In the 160 pixel period of time that the VRS system is being loaded, the video memory actually performs 11 video hardware memory cycles; ten cycles plus another to cover the pipeline effect of the access time delay.

After all of the VRS display data has been loaded, the PAL (pin 17of U231) generates an INIT(L) signal to reset all of the counters and state latches within the VRS system. As the VRS time is about to start, the PAL generates another signal at pin 16, U231, which triggers flip-flops U230A and U230B to generate the start signal CNTE (counter enable) at the proper clock edge. At the end of the VRS display time, U231 generates a pulse at pin 15 that resets flip-flops U230A and U230B, and removes the CNTE signal.

The MUART stage generates a variety of signals that allow microprocessor control of the VRS system. The SCALE(L) signal, U231, pin 9, that sets the current scaling factor for the incoming waveforms also drives U125, pin 39, which is the AXMD (axis mode) signal. This determines the number of axes to place upon the screen, one or two. The BLANK(L) signal, U125 pin 47, allows the microprocessor to blank the video output of the Display Controller Board circuitry. If the BLANK(L) signal is active, all the video outputs will be driven low. The VRS signals CMPD and DIND (U125, pins 44 and 52) for Color Map Data and Diagnostics Input Data,

U700a and associated circuitry detects the relatively small rising transition as a result of the IRLED's coupling light to the phototransistors. Feedback diode CR700b allows U700a to have very high gain in the positive direction and unity gain in the negative direction to achieve high sensitivity and still have adequate response time.

U700b and the four associated resistor shift the 0 to -5 volt levels from the previous stage to TTL compatible levels.

Touch Panel Address Generator

U213 (Front Panel Control Board) generates the 6 bit address bus that is used to select an infrared LED and its compliment phototransistor on the Touch Panel Board.

U211 buffers the Touch Address bus before leaving the Front Panel Control Board.

Clock and Control Generator

U111 and associated resistors and capacitor generate a squarewave at approximately 90 kHz that drives U103 and U114 clock inputs.

U210a generates a pulse called "Sync" that is used to synchronize the Touch Address bus to the 8279 (U103) on the falling edge of /CNT7 from the select lines SL0-SL2 on U103. This trailing edge triggers the one-shot that generates a 500 nS wide pulse.

Along with clearing counters U213a and U213b, this sync pulse causes a value of 7 to be loaded into the clock generator U114, which skews the Touch Addresses ahead by approx 70 µs. The reason for the skew is that the 8279 inherently samples the data on the selected Return Line at the CENTER of it's count duration which results in wasted time following the sample that could be used to set up the analog multiplexers next selection. It also allows more time for the turn on delay of phototransistors.

InfraRed Enable pulse (/IREN)

This pulse ultimately turns on the selected Infrared LED on the Touch Panel Board. U113a, U115b, and U212c use various clocks from U114 to generate the Infrared Enable pulse. /IREN goes active (low) 50µs before U103 samples the selected Return Line. This allows ample time for the phototransistor to turn on and stabilize.

The /Sync inputs to U113 ensures that the flip flop's start and stay in proper phase.

The /IRDIS input to U212c is used for diagnostics to disable the /IREN pulse which inhibits all IRLED's from turning on. This gives the ability to check that all Touch zones change states showing there are no shorted runs and/or phototransistors.

Latch Enable pulse (/LEN)

This signal causes the incoming serial data (SDATA) to be latched into the selected registers of U1001 The 8279 requires that all eight return lines be held stable until the last return line (RL7) is sampled, at which time the byte is loaded into the Sensor RAM. Although the data is dumped into the RAM a byte at a time, each incoming bit is individually compared with the same bit already stored in RAM. If a difference is found, the 8279 sets an internal flag that enables the IRQ line to be asserted when the current scan is completed.

The rising edge of /LEN occurs at the same time the 8279 samples the selected return line.

Soft/Hard key Decoding

For this section, refer to the "8279 Sensor Memory Array" table in the back of this document when necessary.

The first 8 bits (byte 0) are unused because of a problem inherent in the 8279.

U760 and U761 on the Touch Panel board decodes the next five bytes, 1 through 5, and are mapped to the X and Y axis of the touch grid.

Byte 6 is used for the Major Menu Hard Keys and are decoded by U761 on the Touch Panel Board.

Byte 7 is decoded on the Front Panel Control Board by U212a and enables the 74LS151 to route the Front Panel button Board Hard Key states to the 8279.

Menu Status LED Drivers

The Major Menu LED light bars are driven by the display refresh register outputs of the 8279 (on the Front Panel Control board). Internally there is a block of display RAM organized as eight by eight bits. With respect to the "8279 LED Display Memory Array" table in the back of this document, the display RAM is scanned column by column, automatically, lighting the appropriate LED bar(s) when a high bit is encountered. U200, U203, and U214 allow blanking with /BD signal during switching and drive the transistors in U205 and U216 that sink the LED current.

80286 to A Hardware-Software Interface

8279 Modes and Commands:

The following commands program the 8279 operating modes. All commands are sent to the control register at address 3302H. All data is read from or written to address 3300H.

Initial setup

Keyboard/Display Mode Set—04H

Keyboard mode—This input mode is set to "encoded scan sensor matrix".

Display mode—This output mode is set to "8 8-bit character display, left entry".

Thus, after power up and/or RESET, a value of "04" should be written to the control register to set these modes.

Program Clock—22H

This internal clock prescaler should be set to a value of 2, thus, a value of "22" should be written to the control register only after power up and/or RESET.

Display Blanking—A0H

This value should be sent to the control register initially to prevent the display outputs from powering up in the blanked state.

Clear command—C1H

Writing this value to the control register clears all bits in the display RAM and resets the Sensor RAM pointer to row 0. It also resynchronizes the internal timing chain. When this command is used, no data can be written to the display RAM for 160 μs.

Touch Panel and Hard Keys

Read Sensor RAM —50H

In order to read the contents of the sensor RAM, this command must first be written to the control register. Upon receiving an interrupt, writing a value of "50" sets the first read to be from the first row of RAM and sets the auto-increment flag so that each successive read wil be from the next row of RAM. To read all 64 bits of Sensor RAM, make 8 consecutive reads from the data register after writing this command. Refer to the tables and front panel drawing in the back of this document to relate memory bits to actual physical screen locations.

Once the "image" changes and the 8279 asserts the interrupt line, further writing into sensor RAM from the Touch matrix and Hard Keys is inhibited until the interrupt line is reset.

End Interrupt—EOH

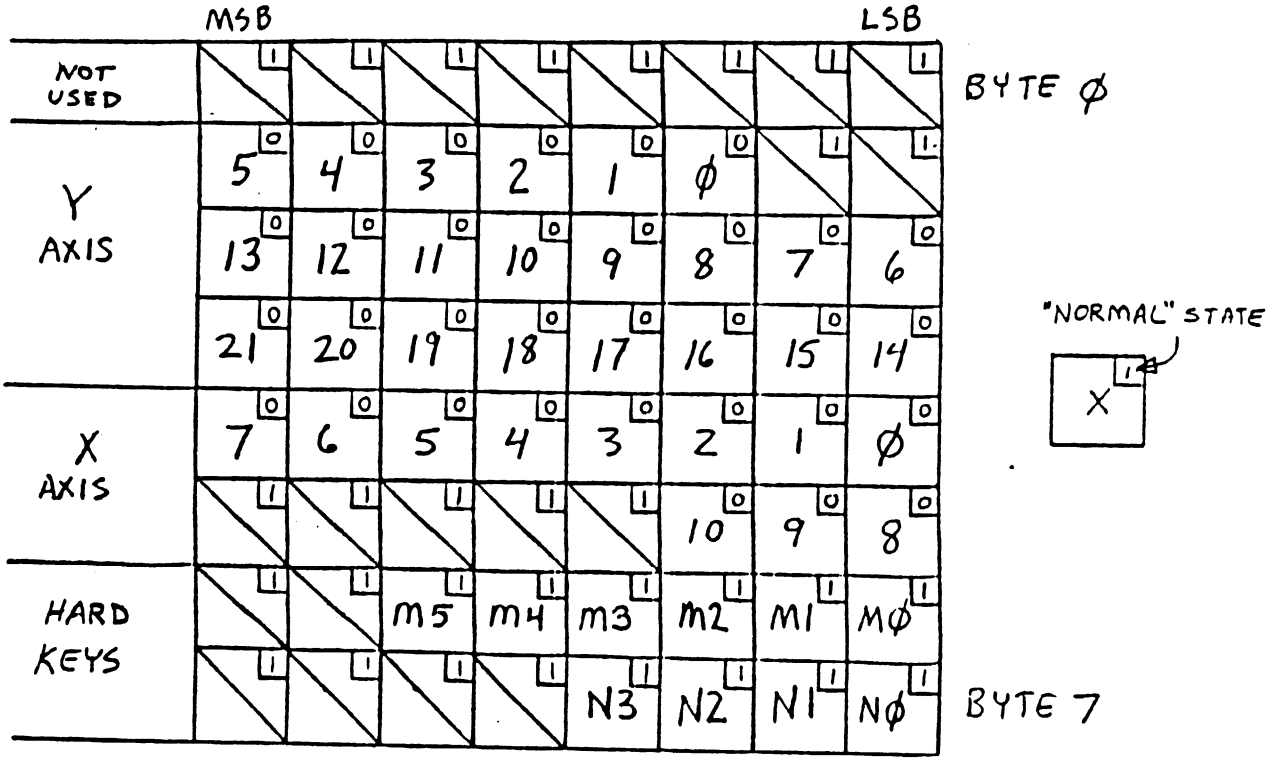
Writing and "EO" to the control register resets the interrupt line, usually after reading the Sensor RAM contents.

Menu Status LED's

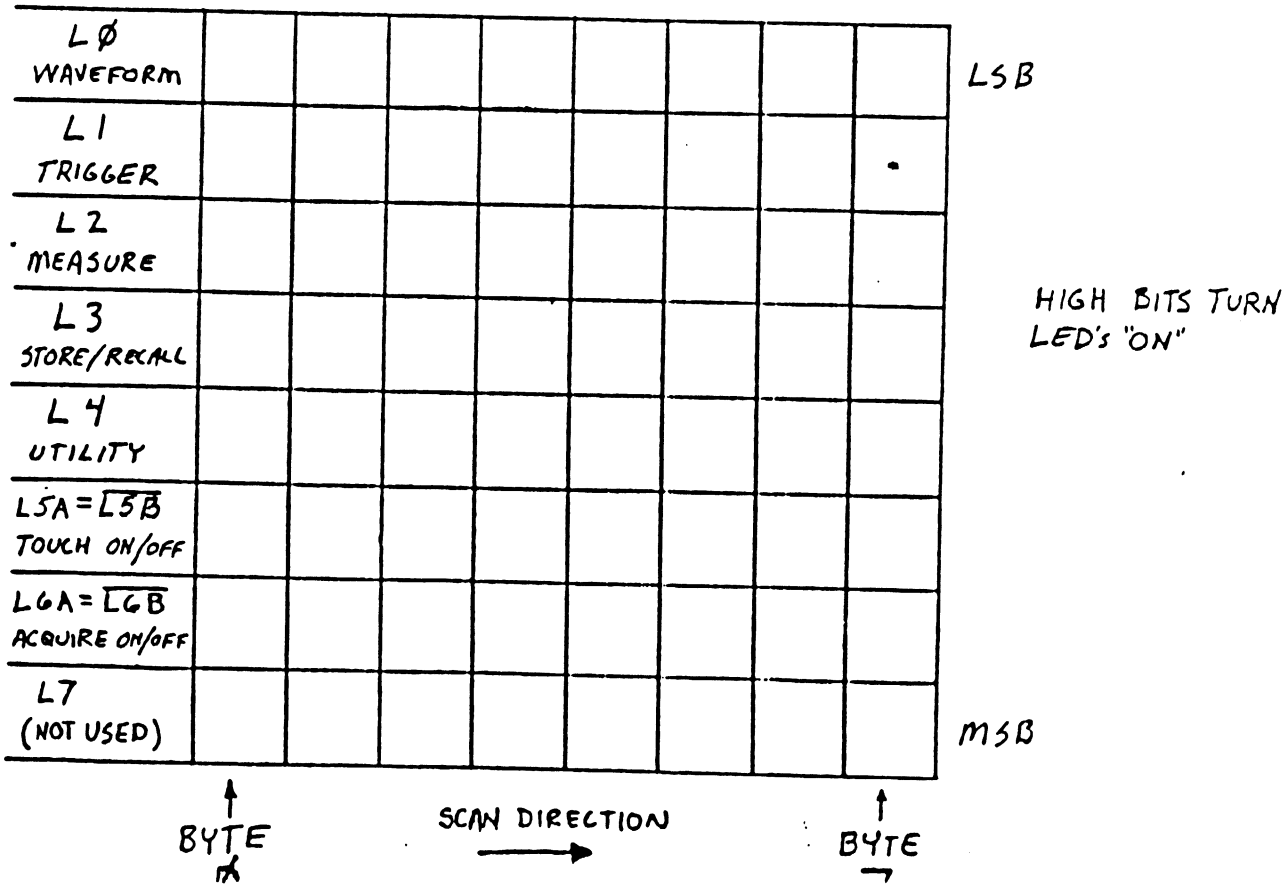
Write display RAM—90H

The EXP sets up the 8279 for a write to the display RAM by first writing this command. Writing the value "90" to the control register places the first data write into the byte 0 column and sets the auto-increment flag such that all subsequent data writes will be to the next column of display RAM. With respect to the "8279 LED Display Memory Array" table in the back of this document, the LED's are scanned from left to right. The LED's turn on with a high in RAM, so, for full intensity, set all eight bits to 1's in the appropriate row.

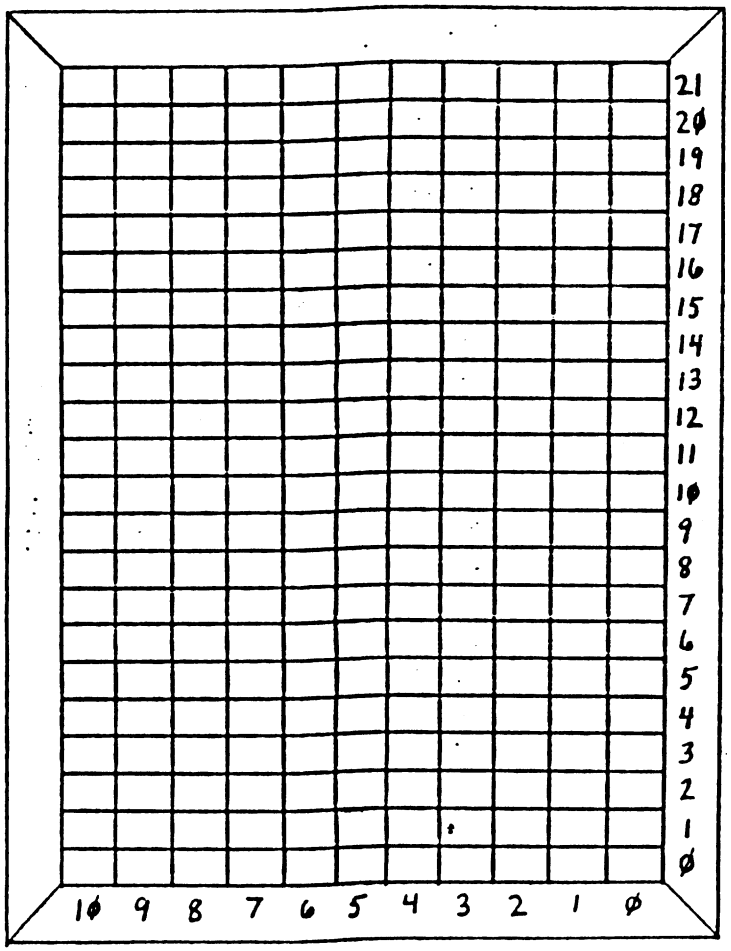
8279 SENSOR MEMORY ARRAY



8279 LED DISPLAY MEMORY ARRAY



TOUCH KEYS, HARD KEYS, MENU LED'S — PHYSICAL LAYOUT



WAVEFORM L0 M0

TRIGGER L1 M1

MEASURE L2 M2

STO/RECALL L3 M3

UTILITY L4 M4

TOUCH PANEL

ON L5A

OFF L5B M5

L6A
L6B N0 ACQUIRE

N1 AUTORANGE

N2 HARDCOPY

N3 ACCURACY

LEFT PLUG-IN

CENTER P-1

5J

9-12-85 B-PHASE TOUCH PANEL (ET)

Bob Simpson – 3

the System Bus by setting the HLDA (Hold Acknowledge) line high. The DMA sets the –GPIB GR (GPIB Grant) line low to tell U410 the DMA is talking to it. Then U410 sets GPIB RQ low. The data transfer takes place over the System Bus, either a read or a write. (At present, the DMA is only used to write to U410.) When the data transfer is complete, the DMA sets the –GPIB GR line high and returns the System Bus to the microprocessor.

The two diode packs (CR602, CR603) are connected to each of the signal lines on the GPIB Bus. They protect the GPIB Bus drivers (U500, U510) from static discharge damage.

The Standard RS-232 Controller (U311) is connected to the same Data Bus and Address Bus as the GPIB Controller. RPD to RPDO transfers data to and from the microprocessor. RPA1 to RPA4 address lines are used by the microprocessor to select individual registers in the Cotnroller. The –STD RS SEL line goes low when the microprocessor wants to communicate with U311. (This line drives the Chip Enable on U311.) The –RD and –WR signals are driven by the microprocessor tosignal if U311 is to be read or written. U311 can requst service from the microprocessor by setting the –STD RS INTR (interrupt) line low. The microprocessor can transmit data on the RS-232 bus by writing a byte into the Controller's transmit buffer. The microprocessor can receive data from the RS-232 bus by reading a byte from the receiver buffer. The microprocessor can also read the status of U311. The RS-232 Conrtoller translates the parallel data from the microprocessor to serial data on TXD RS-232 Bus. It also converts the serial data from RXD on the RS-232 Bus to parallel data for the microprocessor. U310 and U210 are transmit and receive buffers which are compatible with the RS-232 Bus. Clear To Send (CTS) and Data Set Ready (DSR) are RS-232 control signals that can be controlled by the microprocessor. Request to Send (RTS) and Data Terminal Ready (DTR) are signals that can be ready by the microprocessor. Received Signal Detect (RSD) is always high when power is on. This RS-232 port is a DCE type.

Two diode packs are connected to all the signal lines on the RS-232 Bus. The diodes clamp the lines to a maximum of + or –15 volts. This is to protect U210 and U300 from static discharge to the external connector or cable.

The Printer Port (J111) is controlled by a Programmable Peripheral Interface IC (U430). This IC has all the control lines necessary to connect to a microprocessor, plus 2 general purpose 8 bit ports and the control signals to use them. The Rear Panel Data Bus and Address Bus connect to U430 and have the same function as described for the GPIB and RS-232 Contorllers. The –Printer Sel line is set low by the microprocessor when it is communicating with U430. The –RD and –WR lines allow the microprocessor to either read or write to the registers in U430. U430 is initialized by the microprocessor for Port A to be a strobed output prot and Port B to be a storbed input port. Port C provides the control signals.

To send a byte to the printer, the microprocessor writes the byte to U430's Port A. The data appears at Port A and passes to a buffer IU520) and on to the printer port (J111). Next the Port A Output Buffer Full (–OBF) signal goes low and triggers a one-shot (U330A) which triggers a second one-shot (U330B). U330B pin 12 then pulses low for 1 µs. This is buffered by U541 which drives the printer Data Strobe (–DS) signal. When the printer receives the Data Strobe and is ready for the next byte, it returns an Acknowledge (–ACK) signal to U541-8. This then drives U430-11 (Port A acknowledge signal). This completes the handshake of the Printer Controller with the printer. U430 now sets its pin 17 (INTR) high. This signal is inverted by U610C and becomes an interrupt to the processor to tell it the printer is ready for more data.

This Printer Port can also be put in a test mode which causes the data going out through U520 to return through U540 to U430's Port B. This is done by setting U430 pin 13 (NOR/TEST) low. This enables U540. Port B of U430 handshakes with Port A of U430 when this port is set in test mode.

When the printer port is in normal mode (U430 pin 13 high), the printer status is available through Port B. The status information from U541 is strobed into Port B by the microprocessor setting U430 pin 12 (SSTB/INP) low then high. This signal goes through U610B to U430-16 (-STB for Port B).

All the signal lines on the Printer Port (J111) are connected to two diode packs (CR605, CR606). These clamp the lines at the maximum of 0 and +5 volts. This is intended to protect U520, U540, U541 from static discharge on J111.

ET Series 100
Rear Panel Board Interface J78:

Pin Number	Signal Name	Full Signal Name	Definition and Use
1	-RESET	RESET NOT	System reset from microprocessor board. Used to initialize IC's on the R.P. Board.
2	DO	DATA LINE 0	Bidirectional data bus, buffered from the microprocessor Bus. Used to communicate with the microprocessor.
3	D1	DATA LINE 1	Same as above (SAA1).
4	D2	DATA LINE 2	SAA1.
5	GND	GROUND	Power supplies and signals return path.
6	D3	DATA LINE 3	SAA1.
7	D4	DATA LINE 4	SAA1.
8	D5	DATA LINE 5	SAA1.
9	GND	GROUND	Power supplies and signals return path.
10	D6	DATA LINE 6	SAA1.
11	D7	DATA LINE 7	SAA1.
12	-4MCK	4 MHz CLOCK	Clock to drive the GPIB IC.
13	GND	GROUND	Power supplies and signals return path.
14	A1	ADDRESS LINE 1	Buffered and lached address line from the microprocessor. Used to select the registers inside the LSI ICs (UART, GPIB, etc.).
15	A2	ADDRESS LINE 2	Same as above (SAA2).

16	A3	ADDRESS LINE 3	SAA2.
17	GND	GROUND	Power supplies and signals return path.
18	A4	ADDRESS LINE 4	SAA2.

ET Series 100
SDI Plug-In Communications Interface J90:

Pin Number	Signal Name	Full Signal Name	Definition and Use
1	+15 V	+15 VOLTS	This is the +15 volt supply to the Card Cage. Its source is the Plug-in Interface board.
2	L.SDI.CK	LEFT SDI CLOCK	This clock drives the Left Plug-in compartment's serial communications port. Its source is the Std. I/O board.
3	-15V	-15 Volts	This is the -15 volt supply to the Card Cage. Its source is the Plug-in Interface board.
4	R.SDI.CK	RIGHT SDI CLOCK	This clock drisves the Right Plug-in compartment's serial communications port. Its source is the Std. I/O board.
5	PU/-D	POWER UP/ -DOWN	When this line is high, the power supplies are up and regulating. When it is low, it is an early warning that the supplies are going down or are down. The source of the signal is the power supply via the Plug-in Interface board.
6	L.D. PI>MF	LEFT DATA, PLUGIN TO MAINFRAME	This is a serial data path.Data flows from the left plug-in to the mainframe to request setup info and to return its status.
7	GND	GROUND	This is predominantly a signal return path, although supply currents return here too.
8	L.D. MF>PI	LEFT DATA, MAINFRAME TO PLUG-IN	This is a serial data path. Data flows from the mainframe to the left plug-in to control it and ask for status information.
9	R.D. MF>PI	RIGHT DATA, MAINFRAME TO PLUG-IN	This is a serial data path. Data flows from the mainframe to the right plug-in to control it and ask for status information.
10	GND	GROUND	This is predominantly a signal return path, although supply currents return here too.
11	A.D.	AUXILIARY	This is a serial data path. Data flows from the

	PI>MF	DATA PLUGIN TO MAINFRAME	aux. plug-in to the mainframe to request setup info and to return its status.
12	R.D. PI>MF	RIGHT DATA, PLUGIN TO MAINFRAME	This is a serial data path. Data flows from the the mainframe to request setup info and to return its status.
13	GND	GROUND	This is predominantly a signal return path, although supply currents return here too.
14	A.D. MF>PI	AUXILIARY DATA MAIN-FRAME TO PLUG-IN	This is a serial data path. Data flows from the mainframe to the aux. plug-in to control it and ask for status information.
15	A.SDI.CK	AUXILIARY SDI CLOCK	This clock drives the Aux. Plug-in compartment's serial communications port. Its source is the Std. I/O board.
16	GND	GROUND	This is predominantly a signal return path, although supply currents return here too.
19	-RD	READ NOT	If this is low, the selected LSI IC is being read by the microprocessor. It should put data on the data bus (DO>D7).
20	-WR	WRITE NOT	If this is low, the selected LSI IC is being written to by the microprocessor. It should store the data from the data bus on the rising edge of -WR.
21	GND	GROUND	Power supplies and signals return path.
22	DBIN	DATA BUS IN	If this is high, the GPIB IC is being read by the microprocessor or if it is low during a DMA grant to the GPIB, the GPIB IC is being read by the DMA. It should put data on the bus. (See #24 below).
23	-GPIB.RQ	GPIB REQUEST NOT	If this is low, the GPIB IC is requesting service from the DMA. It is used for higher speed data transfers.
24	-GPIB.GR	GPIB GRANT NOT	If this is low, the DMA controller is granting service to the GPIB IC. DBIN tells the GPIB if it is a read or a write. (lo – read, Hi – write).
25	GND	GROUND	Power supplies and signals return path.
26	-GPIB.SEL	GPIB SELECT NOT	If this is low, the GPIB IC is selected to communicate with the microprocessor.
27	-STD.RS .SEL	STANDARD RS232 SELECT	If this is low, the standard UART is selected to communicate with the microprocessor.

		NOT	
28	–OPT.RS .SEL	OPTIONAL RS232 SELECT NOT	If this is low, the optional UART is selected to communicate with the microprocessor.
29	–CENTRONIC .SEL	CENTRONIC SELECT NOT	If this is low, the Parallel Interface IC is selected to communicate with the microprocessor.
30	GND	GROUND	Power suplies and signals return path.
31	–GPIB.INTR	GPIB INTER-RUPT NOT	If this is low, the GPIB IC is requesting service from the microprocessor via the interrupt controllers.
32	–STD.RS .INTR	STANDARD RS232 INTERRUPT NOT	If this is low, the standard UART is requesting service from the microprocessor via the interrupt controllers.
33	–OPT.RS .INTR	OPTIONAL RS232 INTERRUPT NOT	If this is low, the optional UART is requesting service from the microprocessor via the interrupt controllers.
34	–CENTRONIC .INTR	CENTRONIC INTERRUPT NOT	If this is low, the Parallel Interface IC is requesting service from the microprocessor via the interrupt controllers.
35	GND	GROUND	Power suplies and signals return path.
36	GND	GROUND	Power supplies and signals return path.
37	≠12 V	+12 VOLTS	The +12 volt power to the RS-232 line drivers.
38	+5 V	+5 VOLTS	The +5 volt power to the ICs on the Rear Panel Board.
39	+5 V	+5 VOLTS	Same as above.
40	–12 V	–12 VOLTS	The –12 volt power to the RS-232 line drivers.

A14 Input/Output Board

The Standard I/O board is an interface between the Executive Processor (EXP) and communications ports (i.e. RS-232-C, GPIB, etc.), devices on the Front and Rear panel boards, and the plug-in units. It also contains the system Timer, the Real Time Clock, the Serial Data Interface device, the Temperature Sensor and the Tone Generator. The EXP reads and writes to these I/O devices and the communication ports at specific I/O addresses. Accesses to these I/O addresses are decoded to produce device select lines which enable the addressed device. Each I/O device is located at an I/O address at least 100*hex* from any other I/O device. Except for the mother board interface, all the interfaces are via these flexible cable connections:

J72—Front Panel Control Board

J77—Main Processor Board

J78—Rear Panel Board

J90—Plug-in Interface Board

The lower eight bits of the Executive Data Bus are used to transmit data to and from the various I/O devices. The EXP uses this byte of data to configure the various I/O devices and to read their statuses. Naturally, only one I/O device can be accessed at a time.

When the DMA Controller (option 4D) is installed on the Main Processor Board, the Standard I/O board handles GPIB operations differently. See the heading GPIB Control for details of the GPIB interface.

I/O Data Buffer (diagram 21)

The lower eight bits of the Executive Data bus from P105 are buffered by the I/O Data Buffer U832. The output is the I/O Data Bus, which drives data to four different on-board devices.

I/O Delayed Data Buffer (diagram 21)

The I/O Delayed Data Buffer interfaces between the I/O Data Bus and the Write Delayed Data Bus. BDEN, WDDEN(L), and OBSEL are NANDed together to enable the buffer. BDEN is a buffered version of the EXP Data Enable signal. WDDEN(L) is activated by the I/O Control circuitry to keep BDEN from immediately turning on the I/O Delayed Data Buffer at the beginning of a write cycle, when the previous bus cycle was a read from another Write Delayed Data Bus device (i.e. Real Time Clock, Timer, or SDI). The devices using the Write Delayed Data Bus are MOS parts and take a long time (100 – 200ns) to turn off their output drivers. The delay ensures that only one device will drive the data bus at a time. The other enable signal input to U520B is OBSEL, which is generated by the Address/Decode Select circuit to indicate selection of an on board I/O device.

Timer Configuration Logic (diagram 21)

The Timer Configuration Logic is comprised of latch U720 and three 2-input data multiplexers built with discrete gates. When the EXP writes to I/O address 3200*hex*, LS4(L) and BIOWC(L) go active and latch the I/O data bus. Some of the latched bits are used to individually configure the way that Counters 1 and 2 are used. This lets the Timer accept different inputs for different system tasks. U712A and B and U714A determine whether 6 MHz PCLK or the Executive bus signal DIAGNSIG is passed to the CLK input of Counter 2. DIAGNSIG is used to signal the occurrence of a diagnostic test or an operation in a test. The results of a tests on Executive bus boards are put onto DIAGNSIG. U714D supplies the Gate input, G2, with either a constant enable or with DIAGNSIG. When DIAGNSIG is selected as the gate, it can allow PCLK pulses to clock Counter 2. This gives diagnostics the ability to determine how long a DIAGNSIG pulse lasts in that the number of PCLK pulses recorded can be used to compute the duration of the DIAGNSIG gate pulse.

The Counter 1 multiplexer consists of U714C, U712C and D and allows PCLK or the output of Counter 2 to be fed into the CLK 1 input. Cascading the two counters provides for longer counts.

The two lowest bits out of latch U720 can be used to invert the outputs of Counter 1 and Counter 2. This is necessary because the Timer can be set in different modes, and some of these result in an active low output when a counter event occurs. The counter outputs must be active high out of U820 to drive the EXP interrupt pins. The inputs and modes of the counters can be changed at any time.

Counter 0 is used by the operating system as a real-time clock based on the constantly enabled 2 MHz Clk input from the Clock Generator. The Counter 0 output is used to clock U812B. On a positive-going edge, the high D input appears on the output as an IR14 interrupt to the EXP. To clear the interrupt from U812B, the system does a read from the Timer Configuration Logic port at 3200*hex*. Counter 0 runs continuously and generates a positive edge interrupt every time it reaches a maximum count. Then Counter 0 resets to zero and continues counting while the EXP services the Timer interrupt.

Real Time Clock (diagram 21)

The Real Time Clock is comprised of U614 and its oscillator circuit. It keeps track of the current time of day, which is set and read by the EXP. The chip select LS9(L) allows access to the internal registers for I/O reads (BIORC(L)) and writes (BIOWC(L)) of date data. The WR input is driven by BIOWC(L) gated with DLYIO to satisfy timing requirement of U614. Jumper J230 is removed for shipment so the lithium battery, BT130 which powers the Real Time Clock when the main supply is off, is disconnected enroute. Instrument setup instructions direct the technician to replace jumper J230. Battery backup switching is built into the chip to sense when the main supply voltage is low, and enable the battery supply.

CAUTION

Lithium batteries can be dangerous when they are discharged too fast, when more than a minute charging current is applied, or when they must be changed, (see the warning on Lithium batteries in the maintenance section of this manual).

C510 can be used to adjust the oscillator frequency. Putting a probe on the OSC IN or OSC OUT lines will cause a shift in frequency. So, to calibrate the Real Time Clock, software must set it

up in a mode to produce a counter interrupt once every second. Then a timer-counter is used to measure the period from a falling edge to the next falling edge while adjusting C510 to set the period to exactly one second. Six internal registers are addressed with the address lines and loaded from the Write Delayed Data Bus with time of day data. Additional registers allow an alarm function to generate an interrupt output when a specific time occurs. The user can enter the local time after battery jumper J230 is in place.

Each time-count register is read to get information on the present time. To do so, a special register address must be read which causes a second set of readable registers to latch the current state of the count registers. A second read of the registers will give the latched time.

Serial Data Interface (SDI) (diagram 21)

The Serial Data Interface (SDI), U330, is a custom chip that provides serial data communication between the EXP and the three plug-in slots and with both Front Panel knobs. It is controlled by the EXP and it interrupts the EXP when a device requires service. The EXP controls the SDI with I/O writes (BIOWC(L)) and reads (BIORC(L)) to I/O address 2000*hex* - 203E*hex*. The PCLK input is clocked with the 8 MHz signal from the on board Clock Generator. Separate address and data buses are used even though the eight data lines are marked as AD.

The plug-in interface allows communication with the various plug-in units which may reside in the mainframe. SDINs and SDOUTs are serial data inputs and outputs, respectively. The current-limiting 100 ohm in-line resistors and the clamping diode packs CR230 and CR231 give protection from damage due to inserting or removing plug-in units with the power on. Pull-up resistors (10 k) are attached to both the inputs and outputs and tied to 5 volts to pull the lines high when no plug-in is installed. These input and output lines can be read internally by the SDI to determine if a plug-in is installed in each slot.

Input SDICLK monitors CLK1OUT, which is half the frequency of the 8 MHz, Pin 2 PCLK input. CLK1OUT is used to synchronize serial data transfers and is buffered by U320C to reduce loading on the SDI chip. To keep the clock polarity the same as CLK1OUT and to keep a shorted clock line on one plug-in from disabling the other three, the clock signal is inverted and buffered separately for each plug-in channel.

I/O Address Latch (diagram 21)

Executive Address bus lines A0 – A7 are latched by U632 when ALE is high and used to drive various devices.

Address Decode/Select (diagram 21)

PALs U722, U732, and U730 are used to generate all chip selects for on-board devices and for devices on the Front- and Rear-Panel Boards. Executive address lines A0 and A8 – A15 and EXP control lines M/IO and COD/INTA are decoded to produce device select lines S0(L) – S17(L).The device select lines and their associated I/O addresses are listed in Table X.X.

Table X.X
I/O Addresses for Device Selects]

PAL	I/O Address	Select Line	Select Name
	2000 – 203E	S1(L)	SDI Sel(L)
		S2(L)	Not Used
U722	3100 – 3106	S3(L)	Timer Sel(L)
	3200	S4(L)	Timer Confsel(L)
	3300 – 3302	S5(L)	Touchpanel Sel(L)
	3400	S6(L)	TP LED Sel(L)
	3500	S7(L)	Not Used
	3600	S8(L)	Not Used
	3700 – 373E	S9(L)	RT Clock Sel(L)
	3800	S10(L)	Tone Gen Sel(L)
U732	3900	S11(L)	Temp Sense Sel(L)
		S12(L)	Not Used
		S13(L)	Not Used
	4100 – 410E	S14(L)	GPIB Sel(L)
	4200 – 421E	S15(L)	RS-232C Sel(L)
U730	6100	S16(L)	Opt. RS-232C Sel(L)
	6200	S17(L)	Printer Sel(L)

The device select lines are latched by U622 and U630 with the bufferedAddress Latch Enable signal, BALE. The buffer outputs reflect the inputs while BALE is high, and the outputs are always enabled by the U420E output. The latched select lines go to on-board devices and to the Rear- and Front-Panel Boards. The Latched Select lines are also gated to produce buffer enable lines for the I/O board (OBSEL), the Front panel board (FPSEL) and the Rear-Panel Board (RPSEL).

The unlatched, device select lines are gated to produce an early wait request for the EXP that will result in one to four EXP clock (PCLK) cycles being added to the current bus cycle. Later, when the latched select lines become valid, they are gated to request a specific number of wait states for the current bus cycle. The signals connected to U430 but not to U522A or U530 produce the default of four wait states inserted after the wait request. DMA0 SEL(L) acts as a chip select for DMA operations on the Rear-Panel Board. DMA0 SEL(L) used to request one wait state for the GPIB controller chip to give it time to export data.

On Board Power Circuits (diagram 22)

The +15 V and –15 V voltages reach the Standard I/O Board via the plug-in interface connector, J90. They are fused by F600 and F602, respectively. The fused supplies are then decoupled with filter capacitors C502 and C701 and connected to the card cage mother board to supply other Executive boards. U300 and U400 generate +12 and –12 volts for the RS-232 line drivers on the Rear Panel board. U110A, VR100, and R112 produce a precise +6.5 volts, which is used as a reference voltage by the Temperature Sensor.

The +5 volt current for the Front- and Rear-Panel Boards is routed through the Standard I/O Board. Fuse F200 (1 A) protects the Rear-Panel Board from overloads. Likewise, F800 fuses the 5 volt current for the Front-Panel Board. The fuses have indicators on the board that point at their output ends for easy functional checks.

Temperature Sensor (diagram 22)

The EXP uses the Temperature Sensor to get a digital reading of the temperature in the instrument. When a specific temperature change has occurred, the instrument automatically recalibrates itself. The circuit consists of the thermal sensing element U130, operational amp U124 and comparator U122. U130 produces an output current that is proportional to its temperature (1μA/° C). This current produces a voltage differential accross precision resistor R134, which sets the gain of U124. The resistor network on pin 3 produces a reference offset voltage (2.45 volts) for U124 which can be calibrated with R110. The Temperature Sensor is calibrated at one temperature and should remain accurate over its range of –27 to 100° C. The accuracy of the 6.5 volt supply and resistors is critical for accurate operation. As the temperature rises, the output of U124 goes more negative. U122 compares the output voltage of U124 with the output of the Temp/Tone DAC.

Comparator U122 senses the output of the opamp and compares it to theoutput of digital to analogue converter (DAC), U212. The pin 4 output of U212 sinks a maximum of 1 mA, which produces –1.27 volts across R130 and on pin 2 of U122. A value of 0 into the DAC causes pin 2 to sink 0 mAs, which produces 0 volts on R130.

The Temperature Sensor is read by the EXP with repeated writes andreads following the successive approximation algorithm. First, a byte of data is written to the DAC at I/O address 3900*hex* with only the most significant bit (IOD7) set high. This produces a voltage which is compared with the output of sensor opamp U124. The result of the comparison is read by the EXP with the Temp/Tone Readback Buffer. The result, high or low, will become the state of the last tried bit. Next, each lower bit is added in turn, converted and compared. When the least significant bit has been tried, the result is the current temperature value.

DAC Data Latch (diagram 22)

Latch U610 latches data from the I/O data bus on the rising edge of BIOWC(L) when LS10(L) or LS11(L) is active. The latched data is fed directly into the D-A converter U212. The outputs are constantly enabled.

Temp/Tone DAC (diagram 22)

The Temp/Tone Digital-to-Analog Converter changes an eight-bit digital number (0 – 256) into a proportional current (0 – 1 mA) on both its outputs. Both DAC outputs are activated at the same time, but the pin 4 output sinks current while the pin 2 output sources current. When a value of 0 is sent to the DAC it sinks the minimum current of 0 mAs on its pin 4 output but sources the maximum current of 1 mA on its pin 2 output. Conversely, the maximum value of 256 into the DAC causes the maximum current sink of 1 mA out pin 4 and the minimum current on pin 2.

Temp/Tone Readback Buffer (diagram 22)

Eight line buffer U612 is connected to the I/O Data bus and used by the EXP to monitor the Temperature Sensor and the Tone Generator. U612 is read at either I/O address 3800*hex* (LS10(L)) or 3900*hex* (LS11(L)) with BIORC(L). IOD7 reads the output of the comparator to determine the fit of the last tried voltage/temperature. IOD6 reads the Tone Generator enable signal. Diagnostics reads the jumpers J710 – J715 for various purposes (two jumpers are used to set the default RS-232 baud rate).

Tone Generator (diagram 22)

The Tone Generator is based on a 555 timer, U220, with a special current driver to trigger it. The timer puts out a square wave whose frequency is inversely proportional to the digital value written to the Temp/Tone DAC. A zero value into the DAC produces the highest tone. The Tone Generator is enabled with latch U700 by driving data line D8 high to I/O address 3800*hex* (LS10(L) active). The trailing edge of BIOWC(L) actually latches D8. A write to 3800*hex* with D8 low resets the Tone Generator and halt the output. A system reset will have the same effect.

The pin 2 output of the Temp/Tone DAC drives a set of tracking current sources in U214. This output has a maximum value of 1 mA when a value of 0 is written to the DAC. U214 generates two separate current flows; pin 8 produces a maximum of 1 mA and at pin 7 the maximum is 2 mA. These two currents track each other in a 1:2 ratio while driving into another pair of current mirrors in U112. Initially, the transistor with its collector tied to the Trigger input of the timer is turned off, so capacitor C230 is charging at a maximum 1 mA rate. When the voltage level on the Trigger and Threshold inputs reaches the threshold it causes the Output to switch high and Discharge to go low. The low Discharge line causes the transistor (6, 7, 8) to turn off making transistor (1, 15, 16) turn on and try to sink twice the current that U214 transistor (8, 9, 10) is supplying. The result is that C230 discharges at that same rate.

The voltage level on C230 follows a symmetrical sawtooth pattern. The slopes of the sawtooth are longer and the output frequency lower for higher DAC values.

The output drives through a 100 ohm resistor to the front panel connector J72 and out to the front panel speaker. The ground side of the speaker is returned to Pin 1 of U220 to reduce inductive spikes from the speaker coil. CR121 also helps minimize inductive kickback spikes by clamping them to one diode drop. Negative voltage spikes can cause the 555 timer to oscillate at a high frequency. C226 is a large bypass capacitor that reduces noise from the high current needed to drive the square wave Output.

Rear Panel Data Buffer (diagram 22)

The Rear Panel Data Buffer interfaces the I/O Data Bus with the Rear Panel Data Bus. The outputs of buffer U100 are enabled by the Rear panel bus enable signal, RPSEL, WDDEN(L) and BDEN. WDDEN(L) provides a delay to protect MOS devices on the Rear Panel Board. Drive direction is controlled by DT/R(L).

Rear Panel Address Buffer (diagrm 22)

Integrated circuit U200 buffers latched address lines LA1 - LA4, and control lines BIORC(L), BIOWC(L), RESET(L) and DACK0(L) to the Rear Panel. These address lines are used to select rear-panel devices directly. DACK0(L) is active only when the optional DMA controller is installed on the EXP. When not used, DACK0(L) is pulled to 5 V by a 10k resistor.

GPIB Control (diagram 22)

The GPIB interface operates one way with the optional DMA Controller installed and a different way without it. Without the DMA Controller, the EXP controls the GPIB just as it controls other I/O devices. The EXP puts the GPIB in a mode where it transfers a byte during each EXP I/O read or write to it. Input requests or "ready for more data" conditions are signaled with GPIB INTR(L), which becomes IR32. DBIN is not inverted by U802B and so, reflects actual EXP read and write commands.

When the DMA Controller (option 4D) is installed, the GPIB interface is set up by the EXP, but the actual transfer is controlled by the DMA Controller. The DMA Controller monitors GPIB service request line GPIB RQ after it is ANDed with DACK0(L). DACK0(L) removes the GPIB request when the DMA Controller acknowledges it to avoid erroneous multiple requests. DACK0(L) also causes U820B to invert the EXP I/O read line BIORC(L), which becomes the GPIB read/write line, DBIN. This signal inversion causes the memory to see a read signal while the GPIB sees a write signal, thus enabling high speed direct memory accesses (DMA). Each data byte takes two processor clock cycles for a complete transfer. DACK0(L) is buffered by U412B to create DMA0 SEL(L) which is used to enable the Rear Panel Data Buffer and to request one wait state from the DMA Controller.

The GPIB interface is clocked with a 4 MHz signal from the on board Clock Generator.

Rear Panel Select and Interrupt Buffers (diagram 22)

U210A buffers the Latched device select lines LS14(L) – LS17(L), which enable particular devices on the Rear Panel Board.

The device interrupt lines from the Rear Panel Board are buffered by U210B before being sent to the EXP interrupt controllers. If connector J78 is removed, the Rear Panel interrupt lines will be pulled high by the 10k resistors tied to 5 volts. This prevents the EXP from being inadvertently interrupted.

Front Panel Data Buffer (diagram 22)

Integrated circuit U600 buffers the I/O Data Bus to the Front Panel Board. It is enabled by BDEN and FPSEL (Front Panel Select) NANDed together. U522B produces FPSEL when any Front Panel device is selected. The inverted EXP signal DT/R(L) determines the direction of drive.

Front Panel Control Buffer (diagram 22)

Front Panel Control Buffer U800 buffers the device select lines LS5(L), LS7(L), and LS8(L). It also buffers address line LA1, and control lines BIORC(L), BIOWC(L), RESET, and IRDIS(L). IRDIS(L) is a latched control signal that disables the infrared detectors on the Front Panel. To disable the infrared detectors, the EXP writes a zero on I/O data bus line IOD0 to address 3400*hex*. IOD0 is clocked into U700B by ORed BIOWC(L) and LS6(L). The IRDIS(L) is set inactive by writing a one to the latch or by an active RESET(L). During diagnostics the infrared detectors are disabled.

A15 Memory Management Board

The Memory Management Unit (MMU) Board coordinates communications among three instrument subsystems; the Display, the Digitizer, and the Executive Processor (EXP). The MMU Gate Array controls each interface with a different set of handshaking and buffer control lines. In addition to the MMU Gate Array, there are sets of data buffers for each interface, two banks of DRAMS for waveform memory, address decode/select circuits and integrated diagnostic control circuitry. The EXP sets the MMU Gate Array to perform transfers by setting bits in a control register called the Status and Mode Register (SMR). It must also load addresses and byte count information into either the Sequential Address Generator (SAG) or the Random Address Generator (RAG), which reside within the MMU.

MMU Gate Array (diagram 27)

The MMU (Memory Management Unit) Gate Array, U210, controls all data transfers to and from waveform memory. Waveform memory has two identical banks of dynamic memory (Even and Odd DRAM), which are fully supported for simultaneous accesses. The MMU Gate Array controls high-speed transfers of waveform data and communication messages between waveform memory and the three subsystem interfaces: The Display subsystem, the Digitizer subsystem and the Executive Processor (EXP). Each subsystem interface is coordinated by a set of handshaking lines tailored to the DMA (Direct Memory Access) facilities of the subsystem.

The MMU Gate Array also provides refresh addresses, strobes for waveform memory, and arbitration of access requests. Arbitration for all waveform memory accesses is ordered as follows:

1. Refresh cycles;

2. Writes to the Digitizer;

3. On a rotating basis, (polled every 40 ns) either

    - Reads or writes by the Display,
    - Reads the Digitizer, or
    - Reads or writes by the EXP.

Status and Mode Registration (SMR)

The EXP controls the MMU Gate Array with the Status and Mode Register (SMR), which is located at the EXP's I/O address 1860*hex*. Figure X.1 shows the layout of the SMR status and control bits. Upon power up, the EXP must initialize the SMR to enable transfers between waveform memory and the Display subsystem (bits 0 and 1) and the Digitizer subsystem (bits 5 and 6). When set, bit 7 allows the EXP to access the normally unaccessible registers, which are associated with the RAG, SAG and refresh counter. Most transfers end with an interrupt bit (bits 2 – 4) being set high. The EXP responds to the interrupt by writing a one to the bit to clear it.

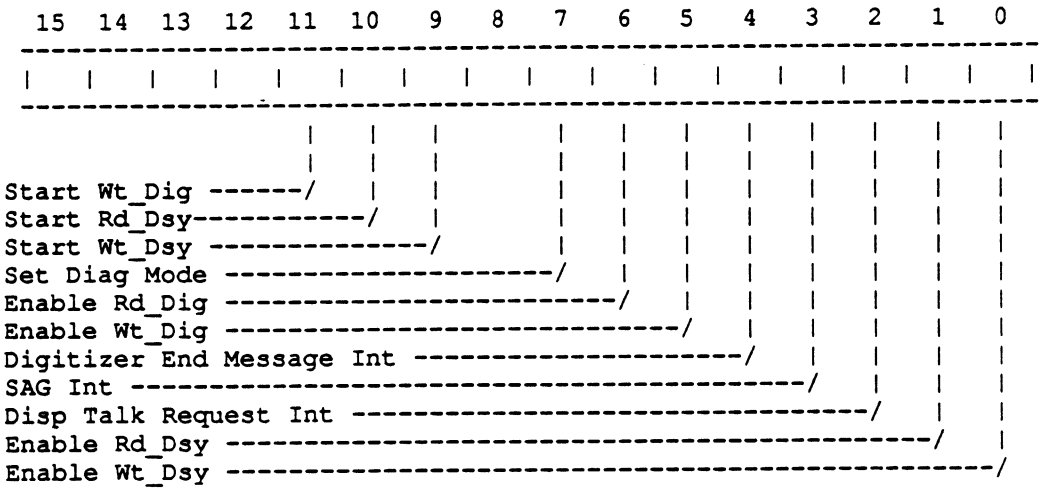


Figure X.1 MMU Status and Mode Register

RAG and SAG Address Generators

Addresses for waveform memory accesses are generated within the MMU Gate Array by the Random Address Generator (RAG) or by the Sequential Address Generator (SAG). The RAG is used only to put waveform data from the Digitizer into waveform memory. Fifteen, nine bit registers, designated RAG0 - RAG14, are the core of the RAG. Each of these, except RAG14, is loaded with a base address for a waveform data record. RAG14 is loaded with an address for communication messages from the Digitizer to the EXP. When the Digitizer is ready to send updated waveform data from an input channel, it sends a four-bit TAG number to specify a RAG register. Along with the TAG number, an offset address is sent by the Digitizer. The RAG adds this offset to the designated RAG base address to determine the memory location for a word of data. Figure X.2 shows a block diagram of the Random Address Generator.

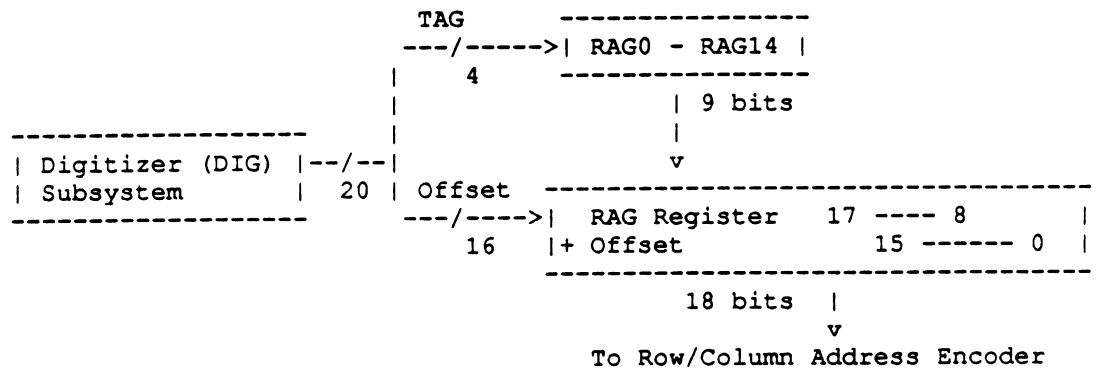


Figure X.2 Random Address Generator (RAG)

The Sequential Address Generator (SAG) is used by the Display and EXP to move large blocks of data into and out of waveform memory and to send messages (from the EXP) to the Digitizer. The SAG consists of a 14-bit Message Pointer Register (MPR) for the base address of a message, a 15-bit Address Counter (AC), and a Message Length Register (MLR). To set the SAG to transfer a message into waveform memory, the EXP first loads the MPR with a beginning address for the waveform record. Next, the AC must be initialized to a value from 0 to 65536 to indicate where in the data block to begin an access. Finally, the EXP loads a value in the MLR that equals the message length plus the value put in the AC. The AC is incremented after each word transfer and compared with the MLR. When the MLR and AC contain equal values the transfer is complete and the SAG interrupt bit is set in the Status and Mode Register. Figure X.3 shows a block diagram of the Sequential Address Generator.

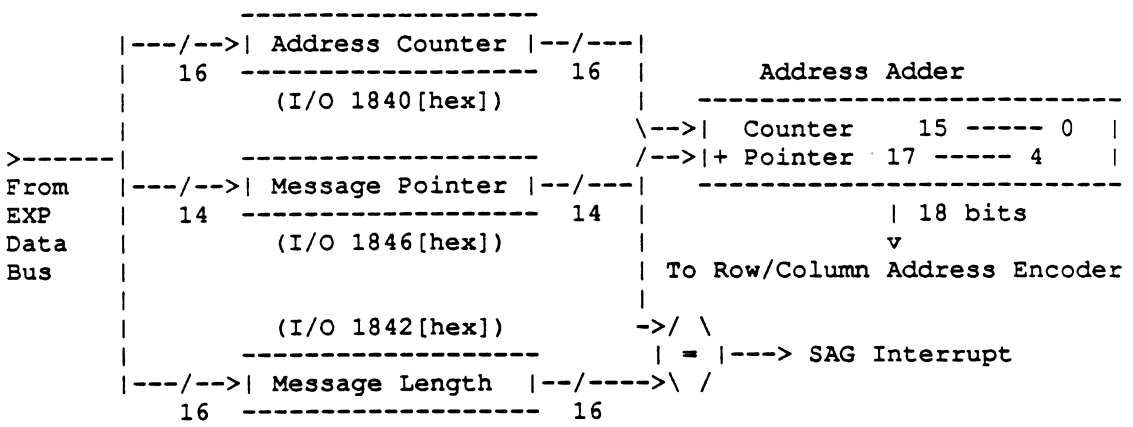


Figure X.3 Sequential Address Generator (SAG)

Display Interface

Data is transferred to and from the Display through the Compressor Board on a 16-bit data bus (Y0 – Y15). These data transfers use the Sequential Address Generator (SAG) to specify the destination or origin addresses in waveform memory. Data is buffered with the bidirectional Display Data Buffers for Even and Odd bank waveform memory accesses. U400B and U500A buffer the four dedicated handshaking lines that synchronize the Display Interface. These buffers can be disabled for diagnostic tests. The special handshaking lines for the Display interface are:

- ENDNEW(L)—Generated by Display to initiate a read of waveform memory. Its falling edge begins a read cycle.
- DATALATCH(L)—Produced by the MMU to clock data from waveform memory into the Display. Data is valid on on the trailing edge.
- DATARDY(H)—Generated by the Display when it is ready to send data to waveform memory.

- DATAGATE(L)—Produced by the MMU to enable, on its falling edge, the Display data buffers during a transfer from Display to waveform memory. Its rising edge signals the end of the Display's write to memory.

Data transfers begin with the EXP setting up the SAG registers. The EXP must have also used the Executive buses to setup the Compressor. To enable a read of memory by the Display, the EXP must set bit nine, Start WT_DSY, in the Status Mode Register (SMR). After bit nine is set, SENDNEW(L) going active will cause the MMU Gate Array to begin a read cycle from waveform memory. Soon after the read cycle begins, the MMU Gate Array will enable the Even or Odd Display Data Buffers and drive DATALATCH(L) low. The trailing edge of DATALATCH(L) latches the data on the Compressor Board or Display Controller Board. These handshake lines continue to toggle and the SAG continues to increment addresses until the specified number of data words have been transferred. At this time, the SAG will set the SAG interrupt bit in the SMR, which generates an interrupt to the EXP. The EXP must reset the SAG interrupt bit to enable future transfers.

A write by the Display into waveform memory follows a similar procedure. First, the SAG is set and bit 10, Start RD_DSY, of the SMR is set. When data from the Display is ready to be sent, DATARDY(H) is asserted. The MMU Gate Array drives DATAGATE(L) low to enable the data buffers at the Display. The low-to-high transition of DATAGATE(L) signals the end of the Display's write into memory. Figure X.4 shows timing for Display Interface read and write cycles.

Figure X.4 Display Interface Timing

Digitizer Interface

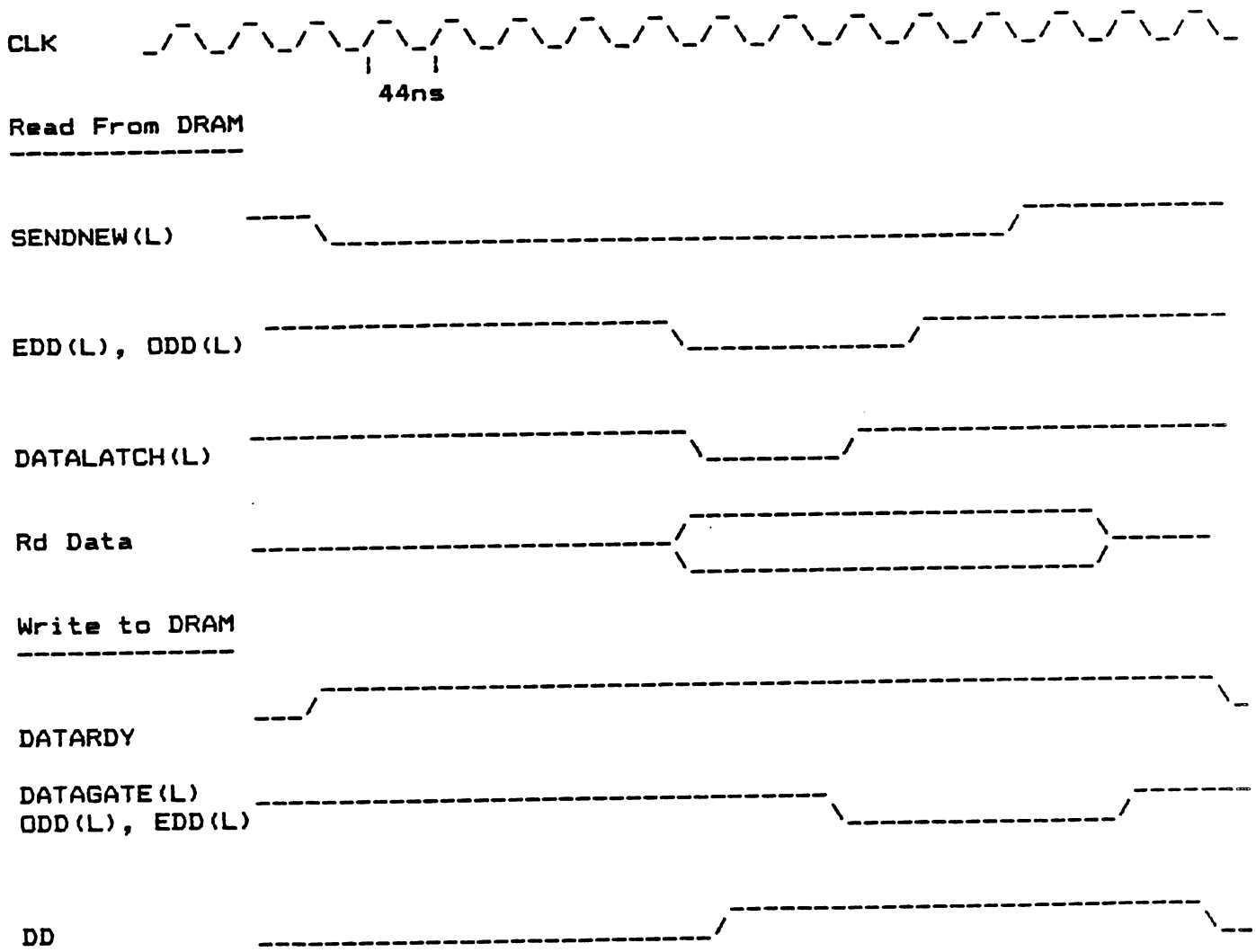
Data is transferred to and from the Digitizer on a 20-line multiplexed address/data bus, which is coordinated by dedicated handshaking lines. For transfers to waveform memory, the Digitizer sends a 20-bit address, then a 16-bit data word. During transfers from waveform memory to the Digitizer, only 16-bit data words are sent while the MMU Gate Array's SAG provides the addressing for waveform memory.

For transfers to waveform memory, the MMU Gate Array latches address bus (G0 – G19) information on the trailing edge of AOUT(L). The upper four bits are the TAG field, which specifies a RAG register for a particular waveform record. The lower 16-bits provide an offset address for each data word in the waveform record.

The interface timing for data transfers from the Digitizer to waveform memory requires the data to be latched by the Digitizer Data Latches. Data is latched when DOUT(L) goes inactive (on the rising edge). These latches, and the Digitizer Data Buffers used for waveform memory reads, are controlled by the MMU Gate Array.

When the Digitizer needs to send acquired waveform data to waveform memory, it asserts DIGREQ(L). (See the timing diagram in Figure X.5.) The MMU Gate Array then asserts AOUT(L) to signal the Digitizer to provide the TAG bits and offset address. The address is latched internally by the MMU Gate Array when AOUT(L) goes high. The MMU Gate Array asserts DOUT(L) to request the release of a word of Digitizer data. When DOUT(L) goes high, the data is latched by the Digitizer Data Latches. Immediately, a waveform memory cycle begins to store the latched data into the waveform memory location specified by the RAG register and the offset address. The Even Bank or Odd Bank is accessed when the Digitizer

Display Interface Timing Figure X.4



address line A0 is 0 or 1, respectively. The appropriate latch output is enabled by ERG(L) or ORG(L) from the MMU Gate Array.

Figure X.5 Digitizer Transfer Timing

Message transfers from the Digitizer to waveform memory are handled differently. The start of a message transfer is the same as a waveform data transfer except that the TAG field for messages is always 0E*hex* for RAG14. When the last word of the message has been sent, a dummy data transfer is sent to RAG15 (0F*hex*), which sets the Digitizer End Message Interrupt, bit 4, in the SMR. No waveform memory cycle occurs for this last RAG15 transfer. Setting bit 4 of the SMR causes the MMU Gate Array to generate an RQS interrupt to the EXP. The digitizer interface locks when another message is initiated before the SMR is cleared.

Transfers from waveform memory to the Digitizer (See the timing diagram in Figure X.5.) operate as follows: First, the EXP must set the SAG with the location of the data and set the SMR START WT_DIG bit (bit 11). Then if the DIGACK(L) line is active or goes active, a read from Even or Odd memory will begin. When data appears on the output of the Digitizer Data Buffers, the MMU Gate Array asserts DIGLATCH(L). This signals the Digitizer to latch the valid data. When, after a number of consecutive cycles, the entire block of data is transferred, the SAG interrupts the EXP.

U501C and U400A buffer the handshake lines and allow them to be disabled for diagnostics. They are disabled with ISO+ (See U400B and U501A). The upper four address lines, G16 – G19, are buffered by the multiplexer U500. U500 allows all these lines to be driven high or low by the diagnostics when ISO– is low.

Executive Processor Interface

The Executive Processor Interface performs two main functions. One is providing the EXP access to waveform memory for subsystem message passing and manipulation of waveform record data. The other main function is to allow the EXP to coordinate system operation by providing access to the Status Mode Register (SMR) and to the diagnostic facilities. The interface consists of address, data, and status/control inputs, EXP interrupt outputs and a data ready output.

Six control lines are decoded by the MMU Gate Array to determine what type of bus cycle the EXP is about to perform. SYSCLK synchronizes the EXP interface, and RESET(L) provides a positive reset on power-up. The input CS(L) is driven active by the Address Decode/Select circuitry whenever the EXP is accessing memory or I/O. The other control and status inputs are decoded for the possible EXP bus cycles in Table X.1.

Digitizer Interface Timing Figure X.5

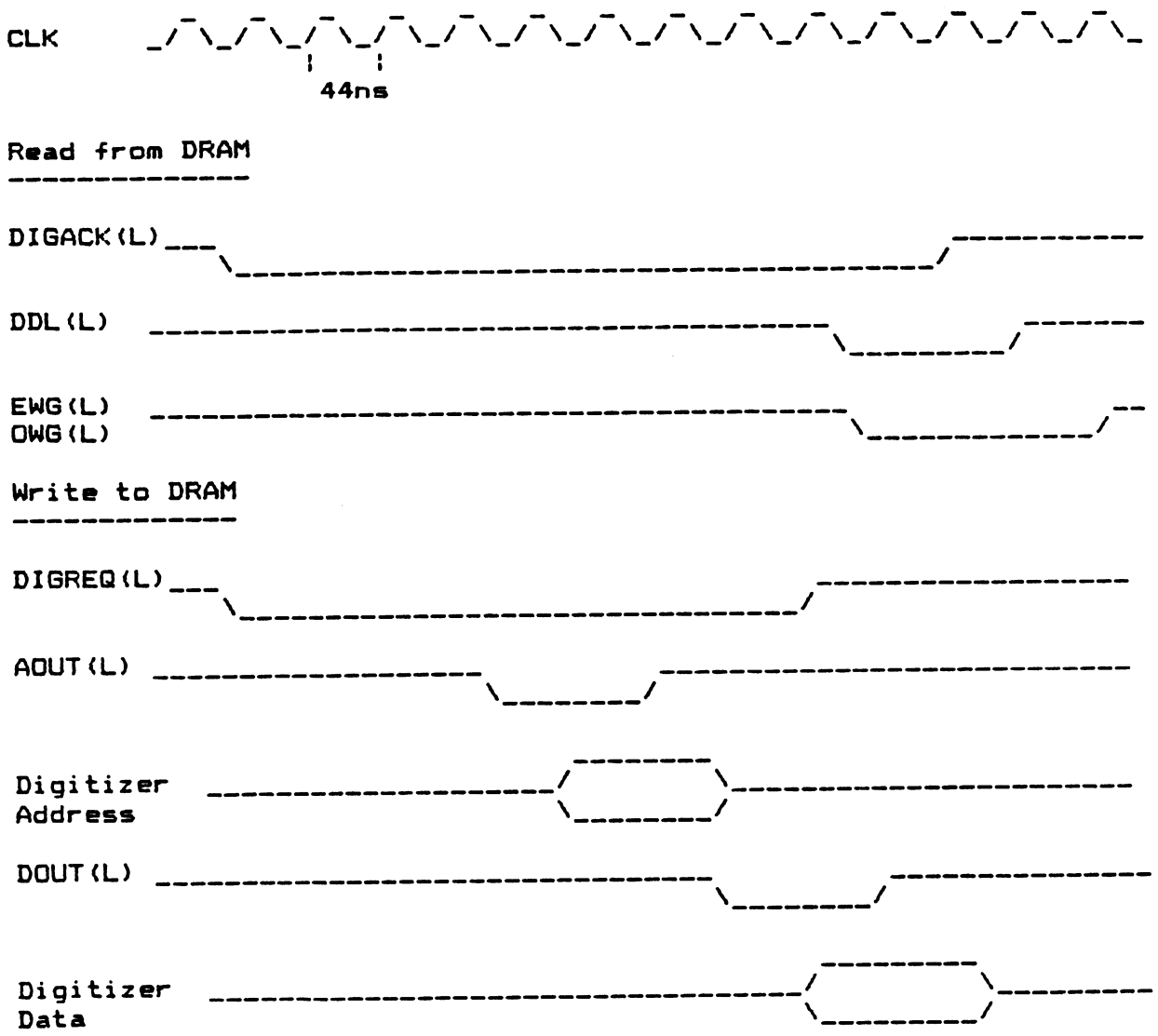


TABLE X.1
Types of EXP Bus Cycles

M/IO	S1(L)	S0(L)	Type of Bus Cycle
0	0	1	I/O Read
0	1	0	I/O Write
1	0	1	Memory Read
1	1	0	Memory Write

BHE(L)	A0	Type of Data Transfer
0	0	Word
0	1	Upper byte valid
1	0	Lower byte valid

If the EXP is to access waveform memory (which appears in the EXP's address space), then SRDY is pulled low by the MMU Gate Array until it is finished with higher priority transfers. SRDY is released near the middle of a memory cycle. The Processor Data Buffers are enabled for the proper direction, then their outputs are enabled. When the EXP is reading waveform memory, the data is latched into the I/O Data Latches with Data Latch Enable until the EXP reads it by activating DEN (Data Enable). Figure X.6 shows the timing for EXP interface cycles.

Figure X.6 EXP Interface Timing

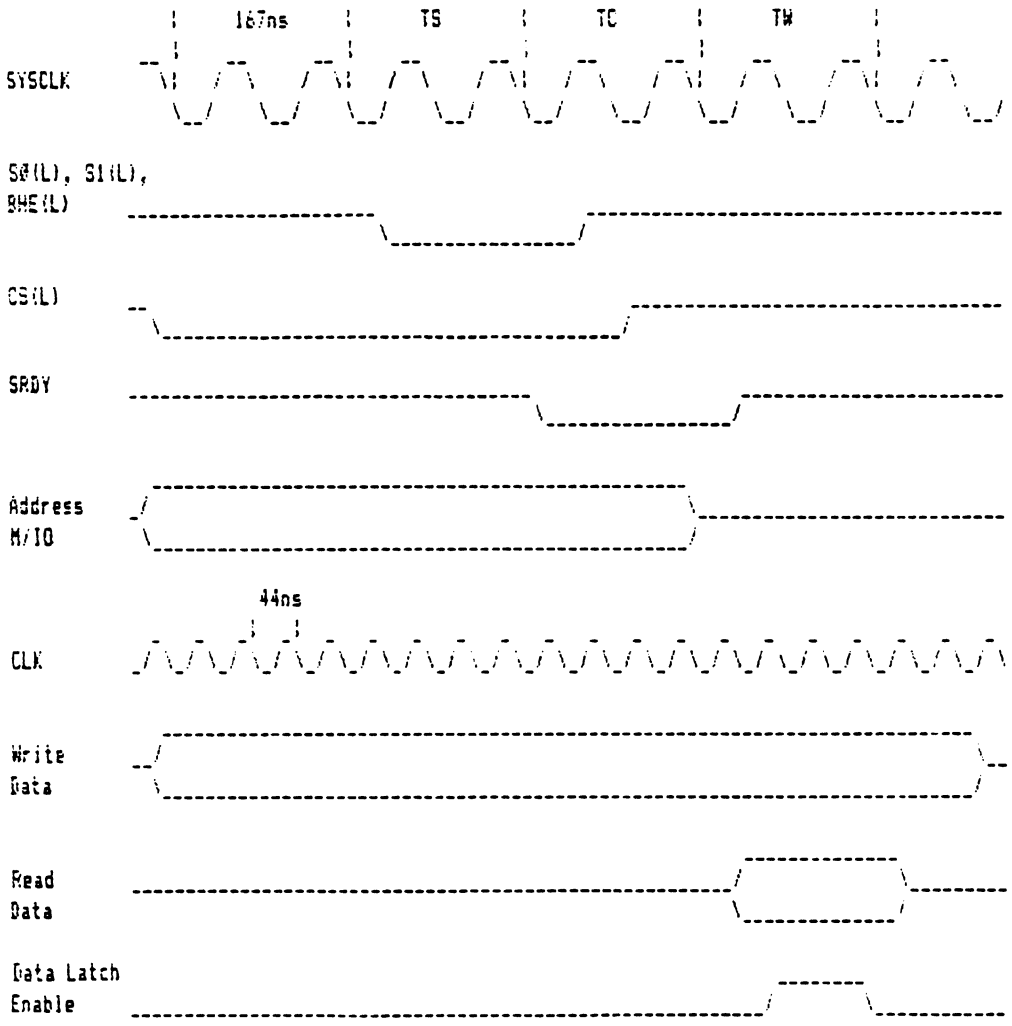
The EXP signal BHE(L) changes only when the next bus cycle is to transfer a different number of data bits (i.e. high byte, low byte or word). SRDY may be held much longer than shown in Figure X.6.

When the EXP is writing directly to the MMU Gate Array, it does so with an I/O bus cycle to address range 1800*hex* – 1FFF*hex*. The SMR is located at I/O address 186*hex*. After a transfer is complete, the MMU Gate Array asserts one of its three interrupts to the EXP. The interrupts are:

- INT0(L)—SAG Interrupt,
- INT1(L)—Digitizer Interrupt (RAG15), and
- INT2(L)—Display Interrupt.

The EXP responds to these interrupts by clearing the interrupt bit in the SMR and, if needed, setting the start bit for another transfer. These interrupt lines are inverted for the Executive bus by U624A-C.

Executive Processor (EXP) Interface Figure X.6



DRAM Control

The DRAM is supported as two separate memory banks (Even and Odd). The MMU Gate Array generates eight-bit row and column addresses for each bank. Each DRAM Column Address Strobe (CAS) controls one byte (two DRAM chips) of memory. This allows for byte accesses by the EXP. The Row Address Strobe (RAS) for each bank goes through a delay line and an OR gate to guarantee proper RAS(L) to CAS(L) timing for the DRAMS. The falling edge of RAS(L) is delayed 10 ns by the delay lines. The rising edge is not delayed because of U110A,C. This ensures that the RAS will be inactive for the required period. The control lines and address lines go through series 33 ohm resistors to provide impedance matching for the DRAMS to protect them from undershoot.

Memory jumper J201 provides for memory expansion Option 2D, which increases memory from 128K bytes to 512K bytes. This is important to the MMU Gate Array when it is generating DRAM address.

Even Dram (diagram 28)

The Even DRAM provides 64 k bytes of dynamic memory for waveform data and for subsystem communication messages. The Even memory is usually accessed alternately with the Odd DRAM. When A0 from either the Display or the Digitizer is low, or when A1 from the EXP is low, the Even bank of DRAM is selected. Therefore, as these address lines go high and low on consecutive addresses, the Even and Odd bank are accessed alternately. The Even bank is divided into a High bank and a Low bank and each of these is further divided into a high-byte bank and a low-byte bank. The MMU Gate Array provides all control signals, refresh signals, and addresses for the Even DRAM. The MMU Gate Array also coordinates data buffers for the three DRAM interfaces (Exp, Display and Digitizer). Of these interfaces, the Executive Processor is the only device that makes byte accesses. Option 2D enlarges waveform memory to 256k bytes by replacing the 16k by 4 bit DRAMs with 64 k by four-bit DRAMs. Figure X.7 shows how the address range for waveform memory is partitioned.

Figure X.7 Waveform DRAM Configuration

Each Even DRAM bank, High and Low, is comprised of two Low byte chips and two High byte chips. The MMU Gate Array generates a separate enable line for each byte chip set. The enable lines connect to the Column Address Strobe, CAS(L), inputs at pin 16. The byte chip sets and their enable signals are:

- High bank—High byte (U422, U420)—C2E(L)
- High bank—Low byte (U430, U424)—C3E(L)
- Low bank—High byte (U322, U320)—C0E(L)
- Low bank—Low byte (U330, U324)—C1E(L)

In addition, the MMU Gate Array supplies the Even DRAM with a common multiplexed eight-bit address bus (J0 – J7), a Row Address Strobe, ER(L), and a write enable, EW(L). The output enables OE(L), pin 1, are tied to ground, but the outputs drive only when a RAS(L) and a CAS(L) have been received. Signal timing is shown in Figure X.8.

DRAM Interface Timing

Figure X.8

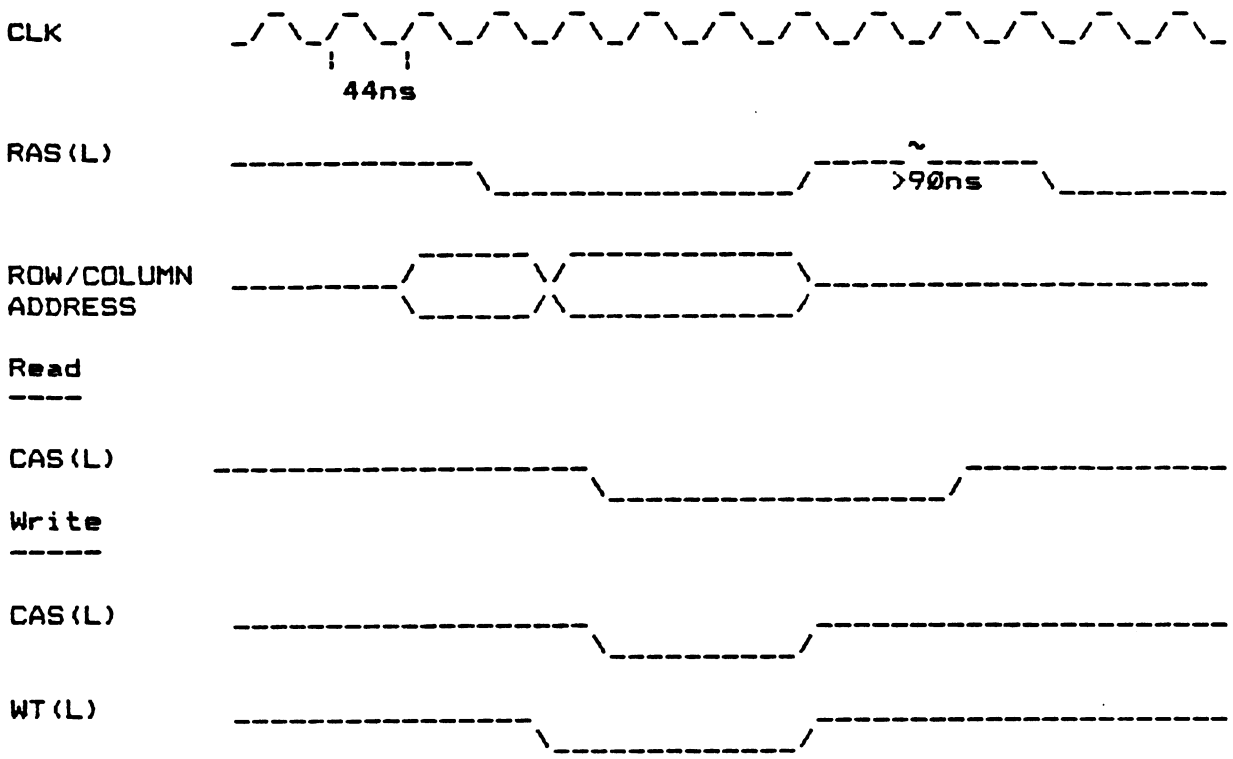


Figure X.8 Waveform Memory Access Timing

Data lines E0 – E15 are shared between the High and Low banks. The Low byte banks share data lines E0 – E7. Likewise, the High byte banks share data lines E8 – E15. All data lines have series 33-ohm resistors to eliminate excessive undershoot on high-to-low transitions. Each data line is also connected through a 2.7 k ohm resistor to +5 volts to pull it high when all drivers are tri-stated.

To address memory locations, the MMU Gate Array sends two consecutive addresses to the RAMs. First the row address is sent on the address lines and latched by the falling edge on the RAS(L) input, pin 5. Then the column address is put on the address bus and latched by a falling edge on the CAS(L) input, pin 16. If the access is to write data into the RAM, the WE(L) input, pin 4, will be driven low soon after the RAS(L) input goes low. RAS, CAS, and WE inputs all return high at about the same time.

Odd Dram (diagram 28)

The Odd DRAM provides 64 k bytes of dynamic memory (248 k bytes with Option 2D) for waveform data and messages. The operation and control of the Odd DRAM is almost identical to the Even DRAM (see the discussion on the Even DRAM for a detailed description). The only differences are the lines that the MMU Gate Array uses to select chips at their RAS(L) inputs:

- High bank—High byte (U222, U220)—C2O(L)
- High bank—Low byte (U230, U224)—C3O(L)
- Low bank—High byte (U122, U120)—C0O(L)
- Low bank—Low byte (U130, U124)—C1O(L)

Also unique to the Odd DRAM are the Row Address Strobe input OR(L), and the write enable OW(L).

Processor Data Buffers (diagram 28)

The Processor Data Buffers interface between waveform memory and the I/O Data Buffers and Latches, which provide data buffering for the Executive Bus. The Processor Data Buffers are eight-line, bidirectional tri-state drivers (the third state is high impedance). There are two sets of buffers; one set, U802 and U702, for the Even DRAM and one set, U812 and U712, for the Odd DRAM.

The buffers are enabled on pin 19 by MMU Gate Array line EEXD(L) for the Even bank and OEXD(L) for the Odd bank. Drive direction for all four buffers is controlled by MMU Gate Array line EXD on the EN inputs, pin 1. When the chips are not enabled, their outputs are set in the high impedance state.

The "B" side of the buffers is connected to the I/O Data Buffers and Latches. MMU Gate Array controlled timing for transfers is shown in Figure X.6 under the MMU Gate Array discussion.

Display Data Buffers (diagram 28)

The Display Data Buffers provide an interface between the Even and Odd DRAMS and the Display system. These Display Data Buffers are eight line bidirectional tri-state drivers (the third state is high impedance). There are two sets of buffers; one set, U610 and U602, for the Even DRAM and one set, U700 and U600, for the Odd DRAM.

The buffers are enabled on pin 19 by MMU Gate Array line EDD(L) for the Even bank and ODD(L) for the Odd bank. Drive direction for all four buffers is controlled by MMU Gate Array line DD on the EN inputs, pin 1. When the chips are not enabled, their outputs are tri-stated.

The "A" side of the buffers is connected to the Compressor Port J79. Figure X.4, under the MMU Gate Array discussion, shows transfer timing.

Digitizer Data Buffers (diagram 28)

The Digitizer Data Buffers drive data from the DRAM memory to the Digitizer through Time Base Port J83. There are two sets of buffers; one set, U514 and U614, for the Even bank and one set, U410 and U510, for the Odd bank. The chip enable CE input, pin 19, for the even buffer set connects to MMU Gate Array signal EWG(L) and the odd buffer set connects to MMU Gate Array signal OWG(L). Figure X.5, under the MMU Gate Array discussion, shows transfer timing.

Digitizer Data Latches (diagram 28)

The Digitizer Data Latches latch data from the Digitizer's multiplexed address/data bus and drive it to the Even and Odd DRAMS. The set of latches, U412 and U512, for the Even bank are enabled by MMU Gate Array line ERG(L) on pin 1. Likewise, the set of latches, U410 and U510, for the Odd bank are enabled by MMU Gate Array line ORG(L). Both sets of latches use the same MMU Gate Array latch enable signal DDL. The "D" inputs are connected to the Time Base Port J83.

Clock Generator (diagram 27)

The Clock Generator is a clocking and a diagnostic circuit that allows the MMU Gate Array clock to be stopped and single stepped. Output of the 23 MHz oscillator Y103 is Anded with the output of D flip-flop U300A and B. The clock signal is inverted by U434C and used to clock in the D input, pin 12, from diagnostic control latch U530. When the D input is low, the Q output, pin 9, goes low. One clock cycle later, the Q output, pin 5, of U300A goes low. This low applied to the pin 10 input of U200C disables the clock to the MMU. While the main clock is disabled, the MMU Gate Array can be single-stepped with the pin 12 input of U110D. This single-step signal comes from diagnostic control latch U530.

Address Decode/Select (diagram 27)

The Address Decode/Select circuitry decodes addresses, control and timing signals from the Main Processor Board (via the Executive Bus) to produce control signals for on-board devices. These on-board control signals either coordinate transfers between the MMU Gate Array and the Executive Processor (EXP) or enable diagnostic hardware.

Digital comparator U232 has a single output that is low when the dynamic Q input matches the static P input. The comparator outputs and some Executive Address and Control lines are decoded by PAL (Programmable Array of Logic) U332 to produce four control signals:

- CS(L)—Active during either an I/O or waveform memory access by the EXP.
- LOE(L)—Active during memory reads by the EXP.
- DIAG(L)—Active when the EXP reads from or writes to diagnostic registers external to the MMU Gate Array at I/O addresses 1900*hex* and 1980*hex*.
- BUFEN(L)—Active during memory and I/O operations to waveform memory or the MMU Gate Array I/O space (1800*hex*-1FFF*hex*).

A group of random logic gates is used to latch and further qualify the PAL control signal outputs. OR gates U432C and U432D distinguish between diagnostic I/O address 1980*hex* and 1900*hex*, respectively. U334 latches the control outputs from U332, U432C and U432D when ALE (from the Main Processor Board) changes from low to high. U434D enables the I/O Data Buffers when DEN is high during EXP operations. U434C enables the output drivers of the I/O Data Latches when the EXP is reading from waveform memory and DEN is high. U720A clocks the diagnostic control latch U530 when I/O address 1900*hex* is written to by the EXP. U432A enables diagnostic buffers U112 and U501B when the EXP reads from I/O address 1980*hex*. U432B enables diagnostic control latch U524 when EXP writes to address 1980*hex*.

Ready Synchronizer (diagram 27)

The Ready Synchronizer circuitry synchronizes the low-to-high transitions of the MMU Gate Array SRDY output with SYSCLK to satisfy a timing specification of the Main Processor Board. SRDY will go low, then high during each Executive Processor (EXP) access of waveform memory.

When SRDY is driven low by the MMU Gate Array and the diagnostic line ISO+ is inactive (low), OR gate U110B will react by driving its pin 6 output low. This low will cause the output of U612A, pin 12, to go low requesting wait states from the EXP. U814B, C and D and D flip-flops U714A and B latch the SRDY low condition.

When the MMU is ready to handle a data transfer, it sets SRDY high, which causes the output of U110B to drive the pin 1 input of U612A high. The Q output, pin 5, of flip-flop U714A will be switching at half the SYSCLK frequency because the output of U814D is high and the toggling feedback to the pin 5 input of gate U814B. When the C input, pin 11, of U714B goes high, it will latch the now high SRDY line to the Q output, pin 9. Pin 9 going high results in the output, pin 12, of U612A going high, which removes the wait request to the EXP. U612B

allows any of the three control lines, RESET(L), ALE, and ISO-, to initialize the Ready Synchronizer and set its SRDY output high.

I/O Data Buffers and Latches (diagram 27)

The I/O Data Buffers and Latches interface the I/O data bus with the Executive Data Bus. I/O reads and writes and writes to waveform memory by the Executive Processor (EXP) employ the bidirectional I/O Data Buffers. The I/O Data Buffers, U724 and U824, drive or receive data according to the level of the DT/R signal, which originates on the Main Processor Board. Chip enable for the buffers is controlled by the Address Decode/Select circuit.

Data Latches U722 and U822 are used only when the Executive Processor is reading data from waveform memory (Even or Odd bank). The MMU Gate Array and DRAM retrieve data before the EXP is ready for it so the data must be latched. Data latching is controlled by a line from the MMU Gate Array. The outputs drive data on the Executive bus when the Address Decode/Select circuit generates the output enable signal. Figure X.6, under the MMU Gate Array discussion, shows transfer timing.

Diagnostics (diagram 27)

Diagnostic support consists of Even DRAM address feedback to the EXP, single-step capability for the MMU Gate Array, and isolation so that handshake lines won't toggle during testing. Several latches and buffers are provided to effect diagnostic control. U530 is at I/O address 1900*hex* for the EXP and must be initialized on power-up to enable normal operation. When used for diagnostics, U530 provides isolation control for the Display and Digitizer handshake lines and the upper four Digitizer address lines (TAG field). It also allows the clock to be stopped and the MMU Gate Array to be single-stepped through Clock Generator control.

The other diagnostic latch and buffer is located at I/O address 1980*hex*. It consists of separate write and read components that carry different information. The write port is U524 which is enabled by the ISO– line and clocked by a line from the Address Decode/Select. U524 allows the handshake lines and TAG field lines to the MMU Gate Array to be toggled for testing. The read port consists of buffers U112 and U501B. When U112 is enabled, the EXP can read the current address on the Even address lines. U501B provides a look at the actual handshake lines from the Digitizer and Display and the setting of memory jumper J201.

A16 Waveform Compressor/Adder

The 11401 waveform display is made of 512 vertical lines. No matter what type of waveform is being displayed, it will always include 512 vertical lines. The length of the individual vertical lines depends on the change in voltage at the time represented by the horizontal location of the particular vertical line. if no input signal is present no vertical displacement of the trace is needed, so the vertical line will benecessarily be longer. The length of the line will represent the ΔV that occurred in the time that this part of the leading edge was sampled.

The Waveform Compressor/Adder (WCA) circuit is one of the circuits the ET main frame uses to produce its display.

The waveform compressor part of this circuit provides 512 pairs of data points to the display. The MU always provides 512 sets of data points to the compressor. Hence, the name "compressor," because the WCA reduces its sets of input data points to pairs of data points.

The pairs of points transferred to the display are the minimum and the maximum of the input set.

The adder part of the circuit provides vertical display position control for the user, by either adding a digital offset to, or subtracting the same digital offset from, the data points.

A normal, nonvectored display may have gaps, or holes, between adjacent points. if the viewer wants a continuous display, without holes, he can select the vectored display.

"Vectoring" takes place by comparing each new data point in a set with a previous pair of displayed values to see if the new point is greater than, equal to, or less than those values.

Vectoring is produced by first:

1. reversing the minimum and maximum values of a pair of points, before calculating the next pair of points,

2. comparing the previous group's minimum with the next group's maximum, and

3. comparing the previous group's maximum with the next group's minimum.

If the previous minimum is greater than the next group's maximum, the next maximum will be considered the same as the previous minimum. This will take the ends of the two adjacent vertical lines end and start at the same point; voila! no gap.

Similarly, if the previous maximum is less than the next group's minimum, the next minimum will be considered the same as the previous maximum. As described previously, the ends of the two adjacent vertical lines will then end and start at the same point.

Figure X.X. To illustrate the concept.

The WCA can transfer data representing displays of any size. The executive processor (EXP) synchronizes the number of points the WCA receives and the number of minimum-maximum (min-max) point-pairs it transmits. To do this, the WCA must receive some number of input points equal to the desired number of ouptut point-pairs times the compression factor (CF).

That is, the ratio of input points to the CF must be an integral value, which equals the number of point-pairs divided by 512.

2. Compressor Modes

The WCA has two modes of operation:

- Transparent (TX). In TX mode, the WCA transfers data directly from the Waveform Ram) to the Display (DSY) without altering it. The data goes through the Compressor and the Adder, and reaches the DSY exactly as it started. Application: messages, i.e., text that must not be changed.

- Compressed (N). In N mode, the WCA selects minimum and maximum values from each group of input data points. The 512 groups of data points each contain N data points, where N = the compression factor.

For example, if the WCA receives 5120 data points, the CF will be 10. This means that there will be 512 input groups of 10 data words each. The compressor will search each of the input data groups, and will produce one min-max pair for each of the 512 groups. The 512 min-max pairs are adjusted by the offset specified in the adder's data register, then sent to the DSY to produce a complete display. (The offset from the ader provides position control.)

3. Compression Factor (CF)

The CF is the number of data points from which each min-max pair is extracted. As shown in Table 1, the CF can be any listed number of 1 to 255. The maximum number of data points that can be compressed and displayed is 130,560 (where [CF][512] = maximum number of data points; and 255 x 512 = 130,560).

TABLE 1

Input Points	Min-Max Pairs	CF
512	512	1
1024	512	2
2048	512	4
4096	512	8
5120	512	10
8192	512	16
10240	512	20
16384	512	32*
32768	512	64*
51200	512	100*
65536	512	128*
130560	512	255*

* = not used in 11401/11402 initial release

"Compressing" Data Points

Compression is the process of selecting the minimum and maximum values from a group of data points. It takes place by comparing all data points in the group and keeping only the minimum and maximum values.

Criteria for Replacing the Minimum

Input data is latched into Min register if:

1. Data is not NULLP and Min is OVER, or
2 Min is NULLP, or
3. Data is UNDER, or
4. Min is not UNDER, and
   Data is not NULLP and not OVER, and
   Min > Data, or
5. Data is last point in group to be compressedd (EOC=true), and
   all NULLP's were found in group (ALLNULL=true), or
6. M/MUND=true.

Criteria for Replacing the Maximum

Input data is latched into Max register if:

1. Data is not NULLP and Max is UNDER, or
2. Max is NULLP, or
3. Data is OVER, or
4. Min is not OVER, and
   Data is not NULLP and not UNDER, and
   Max < Data, or
5. Data is last point in group to be compressed (EOC=true), and
   all NULLP's were found in group (ALLNULL=true), or
6. M/MUND=true.

At the end of the compression sequence:

1. The Min and Max values are transferred into the Adder latches,

2. The role of the Min and Max registers is reversed, i.e.,

   a. the Min register will be the Max register when the next group is compressed, and

   b. the Max register will be the Min register when the next group is compressed,

3. If so specified, set the M/MUND bit true (for nonvectored).

Adder

The Adder provides an offset to vertically positioned the display on the crt. Available offsets range from -32,768 to +32,767, as provided in a two-s-complement 16-bit word. The output of the Adder circuit will be one of the following four cases:

1. NULLP if data is NULLP,

2. UNDER If data is UNDER, or if data is negative, offset is negative, and result is positive,

3. OVER If data is OVER, or if dat is positive, offset is positive, and result has carry, or

4. the sum of the input and the offset.

In Compress Mode, the order within a pair is always first Min, then Max.

Address Decode/Select (U524, U430, & U424, diagram 29)

The Address Decode/Select (ADS) monitors data on the system address bus. During I/O operations, the ADS will respond to a specific address and produce latch enable (LE) signals.

Decoder U524 performs the first stage of decoding; it is wired to produce a low output when its input is 000x 0000 0xxx xxxx on lines A15 through A0, respectively.

When enabled, encoder U430 produces a low on one of its Y0-Y7 output lines, as indicated by the state of the A1, A2, and A3 input lines. Encoder U430 is enabled when:

a. Decoder U524 produces a low on its output;

b. The A12 line is high; and

c. The M/IO(L) line is low.

Latch U424 will hold the ouptut of U430. The ALE signal activates U424.

When ALE occurs with an out-of-range address or for a memory reference, none of the eight selections is valid.

Address bit A4 is not decoded, which results in two I/O address for each selection. For example, address select '0' will be indicated for addresses 1000H and 1010H. Table _-_ shows the address → register mapping.

TABLE _-_
I/O Address Mapping

Location	Operation	Register
1000H	Write	Mode Word
1000H	Read	Status Word
1002H	Write	WCARST*
1002H	Read	ADDATA
1004H	Write	Compression Factor
1006H	Write	Offset
	1008H	Write ROMAX*

* = no register storage

Mode Select Latch (U724, diagram 29)

The WCA Mode Register has three separate mode control bits, which allow eight modes. Each of the eight modes is theoretically possible, though not all are particularly useful. The three mode selections are Compress/Transparent, Vectored/Nonvectord, and Normal/Test.

Compress/Transparent Mode: The C/T(L) bit is used in the adder state machine and the compressor flag-decoding circuit. In compress mode the adder sends the X and Y register values, thus producing two output values for each input group. Special-case flags decoded in the compression cycle are not altered. In the transparent mode, only the X or Y value is sent; that is, just one output for each input group. The special-case flags are forced to be invalid in transparent mode.

Vectored/Nonvectored Mode: "Vectoring" overlaps consecutive group of data. When vectoring is on, consecutive data groups are "comprsesed" with consideration of the previous group's min and max values. With vectoring off, the compressor's X and Y values are marked undefined before operating on a new group. The Vectored/Nonvectored bit is sent to the M/MUND decode circuit.

Normal/Test Mode: This mode specifies whether the adder output is to be transferred to the Display or prsented to the Executive Processor (EXP). In normal mode, the adder state machine waits for the Display's SENDNEW(L) signal before sending the data. In test mode, the adder state machine waits for the decoded DREAD(L) (data read) signal.

Compression Factor Counter (diagram 29)

The compression factor (CF) is the number of dat points from which the compressor will select a min-max pair for the adder. The CF is an eight-bit number, valid in the 1 to 255 range. A value of zero, which is specified as undefined in the HW/SW isnterface for WCA programming, will be equivalent to the value 256. The value stored in the CF register is loaded into an eight-bit counter (U814, U820) by the RSTCYC(L) signal. This counter consists of two four-bit devices (74ALS191) connected as an synchronous two-stage counter with ripple carry-borrow. The RCO(L) output of the lower four-bit counter (U814) is the input to the upper four-bit counter (U820). Both devices are connected as down counters. The MSENDNEW(L) clocks both counters, which provide a Max/Min output when the counter reaches zero. The two Max/Min signals are ANDed to produce the EOC signal for the compressor state machine.

Reset Control (U432D, U130D, diagram 29)

This circuit decodes a Reset signal to set the compressor and adder state machines to known states, and to set, or clear, the control latches. The decoding simply selects the system Reset pulse or an output from the EXP to address 1008H.

Clock Generator (Y122, diagram 29)

A TTL-compatible crystal oscillator, Y122, produces the 20 MHz Clock signal for the compressor and adder state machines.

Compression State Machine (see the Compressor State Machine diagram)

Inputs:

(C)DATAIN(L) (Compressor DATA IN signal, in Compressor Control on diagram 29)

When the MMU latches data into the input register, the (C)DATAIN(L) line is set to its active state (low). The MDATALATCH(L) signal from the MMU clocks D flip-flop (FF) U120A, whose Q output goes low (its D input is grounded). U120A's Q(L) output produces the MSENDNEW(L) signal, which indicates that the compressor cannot receive data while (C) DATAIN(L) is low.

WCARST (Waveform Compressor/Adder ReSeT, in Reset Control, on diagram 29)

The WCARST signal (on TP42) notifies the compressor state machine that a reset is active. In all states, the state machine will change to an initial, known, state when WCARST is asserted. The state machine will stay in that state as long as WCARST is asserted.

EOC (End Of Cycle, from TP47 in Compression Factor Counter on diagram 29)

When the Compression Factor Counter has finished compressing a group of data points, it generates the EOC signal to notify the X and Y Min/Max Latch Decoders (on diagram 2) of that completion. When the most recent input data has been processed, the state machine can follow one of two paths depending on the state of EOC. If EOC is high, the min/max is transferred to the adder input registers. (EOC causes this via U520, U320, U210A, U812, and U510.) If EOC is low, the compressor will assume its idle state, and await the next input from the MMU.

ModeWR (Mode word WRitten, U432A in Mode Select Latch on diagram 29)

Whenever a comprsesor mode word is written into the Mode register, the compressor will pass through its Reset state, asserting the MMUAVAIL and RSTCYC outputs. Writing a new word into the Mode register indicates the beginning of a new transmission through the WCA.

This input is tested only during the compressor's idle state, and it will remain active only for the duration of the EXP's IOWC(L) pulse. Therefore it is specified, in the HW/SW Interface, that a mode word be written only after determining that the WCA is in its idle state. This restriction requires only that the WCA not be restarted while it is transferring previous data.

ADDAV(L) (ADDer AVailable, U224 in Adder Control on diagram 31)

When asserted, ADDAV(L) signifies that the adder state machine is available to accept new data from the compressor. When the compressor has finished compressing a group of data points, it will test its ADDALV(L) input; if neither ADDAV(L) nor WCARST is asserted the compressor will stay in the "wait add" state until one of them is asserted.

Outputs

The variables of the compressor state machine are used as output signals. Each state is represented in a unique combination of state variables.

MMUAVAIL(L) (MMU AVAILable, U222 pin 15 in Compressor Control, diagram 29)

The MMUAVAIL(L) signal has two functions:

- It sets the MSENDNEW(L) signal into the state that indicates the compressor is ready for the next data element from the MMU, and

- It clears the (C)DATAIN(L) input signal.

To speed the executions of the MMU (for fetching the next word) and the compressor (for processing the current input), MMUAVAIL(L) is asserted before the compressor has finished with its current data group. The MMU is specified to take at least 300 ns before it will assert the MDATALATCH(L) control. The compressor state machine will resume its idle state within this 300 ns; therefore, no overrun is possible.

LCTL (Latch ConTroL, U222 in Compressor Control on diagram 29)

Some of the compressor's internal control signals are decoded asynchronously with respect to the state machine cycling. The LCTL pulse synchronizes the ALLNULL and M/MUND signals by latching their values within a compressor state. This stabilizes the control information.

RSTCYC(L) (ReSeT CYCle, U222 in Compressor Control on diagram 29)

The Reset Cycle pulse is produced when the compressor has finished compressing a group of data points. This signal loads the compression factor counter and serves as an input to the M/MUND decoding circuit.

M/MLATCH(L) (Min/Max LATCH, U222 in Compressor Control on diagram 29)

The compressor comparators decode a latch control, and latch the decoded level into a D flip-flop. If the comparator outputs are asserted true (low) the M/MLATCH(L) signal, which is produced after the comparisons have stabilized (being combinationally produced), will cause the Cx and/or Cy LatchEnable signal to change from low to high.

M/MCLR(L) (Min/Max CLeaR, U222 in Compressor Control on diagram 29)

The M/MCLR(L) signal prepares the Cx and Cy registers to receive new data by setting their Latch Enable inputs low.

ADDLATCH(L) (ADDer LATCH, from U222 in Compressor Control, diagram 29)

When the compressor has data fro the adder and the adder is available, the compressor sends ADDLATCH(L) to latch the data from the Cx and Cy registers to the Ax and Ay registers.

IDLE(L) (from U222 in Compressor Control on diagram 29)

The IDLE(L) signal indicates that the compressor is in its idle state. IDLE(L) is connected to the compressor status word registers. Indicating that the compressor is idle ensures that the compressor has finished processing the information it received from the MMU.

NOTE

When the compressor is in idle state, the (C)DATAIN input will occur asynchronously and will cause the state machine to change states. The state, to which the machine goes after idle, should be only a single bit different from idle (or

an indeterminate state may exist). Therefore, the idle bit will be asserted one state after the compressor recognizes input from the MMU. This means that the idle flag will be inaccurate for one state period. Such a discrepancy will produce no erroneous operation if the idle bit is tested only after the current transmission to the Display has resulted in an interrupt from the GPAG. This restriction is acceptable because the compressor is known not to be idle between the time an MMU transfer is initiated and completed.

MMU Input Register (U500, U800 on diagram 30)

Data from the MMU is latched into a 16-bit register, which consists of U500 and U800.

The latch control signal, MDATALATCH(L), is derived directly from the MMU DATALATCH(L) signal; it is asynchronous with the WCA clock.

NOTE

U120 inverts data bit 15 at the output of U500; it stays inverted until it is restored before the adder presents it to the display.

Special Case Flag Decoding

The WCA recognizes three special cases of data: Null, Over, and Under. Outside the WCA, three 16-bit words represent these three cases; these three cases are encoded by three mutually exclusive bits within the WCA. These cases directly affect the min/max latch decoding and the selection of the output value from the adder circuit. When a data value is latched into Cx, Cy, or both, the special flags are also latched. Therefore the Cx, Cy, Ax, and Ay registers are effectively 19 bits wide (16 bits of data and 3 bits of flags). Ths recognition circuit is combinational; it settles to the correct state after the MMU input registers is changed. The flags are decoded only in Compress Mode, as previously explained. Four eight-bit identity comparators perform the decoding.

	BYTE	
Comparator	Upper	Lower
#1 recognizes	0111 1111	---- ----
#2 recognizes	---- ----	1111 1111
#3 recognizes	1000 0000	---- ----
#4 recognizes	---- ----	0000 000x

The comgination fo these four comparisons and data bit 0 are used to decode the three special-case flags.

NOTE

In the compressor circuit, the flags are positive true; in the adder circuit they are negative true.

X Comparator and Y Comparator Output Latches (U510, U812, U310 U612 on diagram 30)

These two registers hold the intermediate values of a comprses group's minimum and maximum values. The comparator X register can serve as either the minimum or maximum register, as determined by the M/M MUXSEL signal to U320. The comparator Y register will always be the opposite of X; if X is min, Y will be max, and vice versa. The outputs of these registers are connected directly to the input of the adder registers.

X and Y Comparators (U410, U710; U302, U610 on diagram 30)

These two eight-bit comparators permit the system to compare the compressors' present contents with the current input from the MMU. Each comparator produces four signals, which indicate that (P>Q) (L) and (P=Q) (L) in both the lower and upper bytes. The MMU input register is connected to the P input to the X and Y Comparators, and the X and Y Comparator Ouptut Latches are connected to their Q inputs. The four output signals encode the relation between the values being compared; they are decoded in the min/max latch decoder (U420, U520 on diagram 30).

Upper		Lower		
(P>Q)(L)	(P=Q)(L)	(P>Q)(L)	(P=Q)(L)	Relation
0	0	0	0	Undefined Upper and Lower outputs
0	0	0	1	Undefined Upper outputs
0	0	1	0	Undefined Upper outputs
0	0	1	1	Undefined Upper outputs
0	1	0	0	Undefined Lower outputs
0	1	0	1	P > Q
0	1	1	0	P > Q
0	1	1	1	P > Q
1	0	0	0	Undefined Lower outputs
1	0	0	1	P > Q
1	0	1	0	P + Q
1	0	1	1	P < Q
1	1	0	0	Undefined Lower outputs
1	1	0	1	P < Q
1	1	1	0	P < Q
1	1	1	1	P < Q

X and Y Minimum/Maximum Latch Decoders (U420, U520, U320, and U210A & B on diagram 30)

A combination of inputs (two sets) indicates whether the curent input should be latched as the new minimum or maximum of the current group. The two sets (each set includes comparator, register, and latch) are virtually identical — they differ only in that at one time X will be min and Y will be max, or vice versa. The latch decoding takes place in a programmable array logic (PAL) IC, one for X (U520), and one for Y (U420). These PAL's produce two outputs — one for minimum and one for maximum latching. The two outputs are active low, combinationally derived, and are synchronized to the compressor state machine with a D flip-flop (U210A and B). The requirements for latching are as follows:

Adder Input X and Y Latches (U712, U412, U512, and U312 on diagram 31)

The Input X and Y Latches hold the input values for the adder. The inputs of these latches are connected directly to the ouptut of the compressor's Comparator Ouptut Latches (diagram 30).

Adder Input Multiplexer (U202, U314, U414, U614, and U714 on diagram 31)

This multiplexer combines the output of the two Input X and Y Latches into a world-serial data stream for presentation to the Adder. The RSEL signal from the Compressor Control (diagram 29) controls the multiplexer's operation, thus designating the order in which the data from the inptu data latch reaches the adder. This selection process is necessary to ensure that the data always reaches the adder in minimum, then maximum order.

Adder Offset Register (U624, U722 on diagram 29)

The input data to the adder can have a 16-bit offset included. This offset must be stored in two's complement to allow for both addition and subtraction. The offset is entered as the other operand to the actual adder chips.

Output Word Control (U102A and F, U112A and B, and U114A and B on diagram 31)

The output of the adder is connected to an output word selector. If the input data was one of three special cases (Null, Over, or Sum) in the adder inptut registers, that special case will be transmitted — not the result of the addition. The outptu selector provides the function that selects either the sum or one of the three special cases. The following equations determine the values of S1 and S2, which are like two selector lines for a four-to-one multiplexer.

S1	S2	Select	
1	1	NULL	If AX(AY) is NULL
1	0	OVER	If AX(AY) is OVER, or AX(AY) bit 15 = 1, offset = 0, and carry exists
0	1	UNDER	If AX(AY) is UNDER, or AX(AY) bit 15 = 0, offset bit 155 = 1, and sum bit 15 = 1.
0	0	Sum	Any other condition.

NOTE

If the added sum forces a positive value over the OVERrange value, the output data will be set to OVER. Similarly, if the added sum forces a negative value below UNDERrange, the output value will be set to UNDER.

Adder State Machine (Refer to the Adder State Machine diagram)

Inputs

Test

When the WCA is in Test Mode, the adder "expects" the EXP to read the data normally destined for the Display. The decoded IORC(L) pulse provides the read signal, via U324B on diagram 29.

C/T(L) MODE (Compress/Transparent MODE, from U724 on diagram 29)

When the WCA is in the compress mode, the adder state machine will transsmit both its input values to U100A, B, and C (diagram 2) and U224 (diagram 31) as a min/max pair or points. In the transparent mode, only one value will be sent.

DREAD(L) (Data READ, from U324B on diagram 29)

DREAD(L) Is the decoded data read signal. It is the result of an EXP input operation from address 1002H.

RSEL (Register SELect, from U332B on diagram 29)

RSEL indicates to the adder (diagram 31) which of its two inputs to process first.

(A)DATAIN(L) (Adder DATA IN, from U330A on diagram 31)

When the compressor latches data into the adder input registers, U330A asserts the (A)DATAIN(L) signal. The ADDLATCH(L) signal from the compressor clocks U330A.

WCARST(L) (Waveform Compressor/Adder ReSeT, from U232A on diagram 29)

WCARST(L) notifies the adder state machine that a reset is active. Regardless of its present state, the state machine will change to an initial, known state when WCARST(L) is asserted. The machine will stay in that state as long as WCARST(L) remains asserted.

Outputs

MUXEL (MUltipleXer SELect, from U224 on diagram 31)

MUXEL, the multiplexer control line for the adder input register, is decoded from RSEL.

ADDAV (ADDer AVailable, from U224 on diagram 31)

ADDAV indicates that the adder is idle (ADDAV high = adder idle). A high on ADDAV means that the adder will accept data from the compressor. ADDAV is also connected to the WCA Status word register.

DDATALATCH(L) (Display DATALATCH, from U224 on diagram 31)

The DDATALATCH(L) line coverns the transfer of data to the Display. DDATALATCH(L) also sets the (A)DATAIN line to a low logic level. For more detail about DDATALATCH(L), see the external specification.

DSENDNEW(L) (Display SENDNEW, from the Display (unit)

The Display asserts a low-logic level on DSENDNEW(L) when it wants the adder to send new data to the Display. For more detail, see the external specification.

DATE(L) (DATA Output Enable, from U224 pin 17 on diagram 31)

The DATAOE(L) signal enables the cable buffers which furnish data to the Display.

Display to MMU Transmission

The MMU controls the arbitration of the bidirectional data path between it and the Display. The WCA does not interfere with that arbitration; yet it interacts with it by providing buffers which must be enabled for the Display to MMU path. The buffer enable signal is derived from the DATAGATE(L) interface line. It is delayed by U100D to ensure that the data is valid long enough for the MMU to read it.

A17 Main Processor Board

After the user requests an instrument operation (with a front panel control for instance), the Main Processor Board (MPB) directs the instrument in performing the operation. Another primary function of the MPB is to run diagnostic self tests on the instrument when powering up or when requested by the user. The MPB controls instrument operations by controlling and monitoring the other circuit boards sharing the Executive System Bus. Through the Executive bus boards, the MPB also indirectly controls all other instrument boards. The Central Processing Unit (EXP) generates command and status signals to control on board devices (i.e., Numeric Processor Extension, Interrupt Controllers, Bus Controller), which help process data and help control the rest of the instrument. The Central Processing Unit is referred to elsewhere in the Theory of Operation section as the Executive Processor or EXP.

The EXP effectively controls the system by running firmware routines stored in EPROMs located on the MPB and on the Memory Board. Along with the Numeric Processor Extension (NPE), the EXP does all data processing not directly related to generating the display or digitizing the waveform. When power is first applied to the system, the EXP runs local and system diagnostic tests, which are located in the on-board EPROMs and on the Memory board.

To reduce the load on the EXP, the Interrupt Controllers monitor the many interrupt lines for service requests from other devices in the instrument. When an interrupt occurs, the Interrupt Controllers notify the EXP and supply it with a vector address to a firmware routine to service the interrupting device.

As a system option (Option 4D), a DMA (direct memory access) Controller can be installed on the MPB. The DMA device increases the data transfer rate for the GPIB external interface. When operating, the DMA Controller has full control of the Microprocessor and Executive buses while the EXP is idle in a Hold condition.

The Bus Controller runs the local Microprocessor bus and the Executive bus with optimal bus cycle timing. It adds wait states (additional clock cycles) to the current bus cycle only when they are requested by a system device.

The Clock Generator provides synchronizing clock signals for the MPB and the rest of the Executive boards. It also produces device ready and system reset signals that are in sync with the clock signal.

Central Processing Unit (Exp) (diagram 23)

The Central Processing Unit, U830, referred to hereafter as the Executive Processor (EXP), controls instrument operations by deciding which devices can use the Microprocessor and Executive buses and when. The EXP also processes acquired and stored waveform data. The EXP gets instructions for performing its operations from software stored in EPROMs located on the Main Processor Board and the Memory Board. The EXP controls all Microprocessor Bus and Executive Bus operations, through the Bus Controller, except when the optional DMA controller has been granted control. Peripheral devices (such as the Memory Management Unit or external interfaces) request service from the EXP by generating an Interrupt Request.

The EXP programs and controls the Interrupt Controllers, the Numeric Processor, and the optional DMA Controller. This programming is done at power-up initialization and may also occur during normal operation.

The clock rate of the EXP is 6 MHz, which is derived internally by dividing the CLK input, pin 31 of U830, by two.

The EXP controls on-board devices with a variety of status and control signals The status lines (S0(L), S1(L) and M/IO start each bus cycle and determine its type. Table X.1 lists the possible states of these signals and the names of the associated bus cycles. Bus cycles end when the input READY(L) comes active.

TABLE X.1
EXP Status and Bus Types

M/IO	S1(L)	S0(L)	Type of Bus Cycle
0	0	0	Interrupt Acknowledge
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	Idle
1	0	0	Halt or Shutdown
1	0	1	Memory Read (Instruction Read)
1	1	0	Memory Write
1	1	1	Idle

When /Bus High Enable, BHE(L) (pin 1), is Low it indicates that data will be transferred on the upper eight data lines, MD7 - MD15. /BHE and MA0 together signal whether the next transfer is for a word or for only the upper or lower byte. Table X.2 shows this relationship. Control output Code/Interrupt Acknowledge, COD/INTA, distinguishes between instruction reads from memory reads. (In address decoding, it is used to distinguish between INTA and I/O bus cycles.) If M/IO, S1(L) and S0(L) are low, a low on COD/INTA indicates an Interrupt Acknowledge Cycle. Figure X.1 shows the timing of the status and control lines from the EXP and from the closely tied Bus Controller and Clock Generator.

TABLE X.2
Data Transfer Type

BHE(L)	MA0	Type of Data Transfer
0	0	Word
0	1	Upper byte valid
1	0	Lower byte valid
1	1	Undefined

Figure X.1. Main Processor Board control signal timing.

Four EXP signal lines (PEREQ, PEACK(L), BUSY(L), and ERROR(L)) provide efficient communication between the EXP and the NPE. For the functions and timing of these signals, refer to the discussion of the Numeric Processor Extension.

The Interrupt Controllers monitor the system interrupt lines to ensure that the highest priority interrupt gets serviced by the EXP. When a system interrupt is received, the Master Interrupt Controller asserts the INTR signal line to notify the EXP that an interrupt is pending. The EXP will finish execution of its current instruction before acknowledging and servicing the interupt.

The EXP acknowledges the interrupt by asserting INTA(L) two times in succession. The Interrupt Controllers place a vector address to jump to a software routine on the Microprocessor Data Bus lines MD0 - MD7 for the EXP. The EXP runs the interrupt handling routine, then returns to its previous operations. Figure X.2 shows the Interrupt Acknowledge Cycle timing. For more information on interrupt processing, see the discussion of the Interrupt Controllers.

Figure X.2. Interrupt Acknowledge Cycle Timing.

When the optional DMA Controller is installed, it uses the HOLD and HLDA lines for bus requests and bus grants, respectively. The DMA Controller drives HOLD high when it needs ontrol of the Microprocessor and Executive buses to service a peripheral device. When the EXP is ready to relinquish the buses, it responds by asserting the HLDA line and tri-stating (put in a high impedance state) its address, data and control line outputs.

Numeric Processor Extension (diagram 23)

The Numeric Processor Extension (NPE), U500, is a high-speed floating point procesor that executes instructions in parallel with the EXP. The NPE is programmed and controlled by the EXP as an I/O device at addresses 0F8*hex* to 0FF*hex*. The NPE is enabled at the numeric processor select input, NPS1 (pin 34), by latched select line LS1.

The NPE and EXP share four dedicated signal lines which allow efficient operation and data bus sharing. When the NPE is ready to transfer data it asserts PEREQ, pin 24. The EXP asserts PEACK(L), pin 36, when it is ready to acknowledge the NPE request and generate the necessary address and bus cycle signals. While the NPE is executing a command, it keeps BUSY(L), pin 25, asserted. If the NPE encounters a problem while executing a command, it asserts ERROR(L), pin 26, which interrupts the EXP.

After the NPE has issued a PEREQ and received a PEACK(L), the Bus Controller will generate an I/O read, IORC(L) (MC8), or an I/O write, IOWC(L) (MC9), command. These are received by inputs NPRD(L), pin 27, and NPWR(L), pin 28, respectively, and cause the NPE to begin a data transfer over the Microprocessor Data Bus. Figure X.3 shows the timing of the status and control signals associated with the NPE. A data transfer bus cycle ends when input READY(L), pin 40, is asserted.

The EXP sends control commands to the NPE by enabling it with LS1(L) and by driving inputs CMD0, pin 29, and CMD1, pin 31, with latched EXP address lines LA1 and LA2, respectively. The data lines to the NPE can be driven with data to load its internal control registers or they can be read in order to get control and status register information. Most other signal inputs and outputs are also involved in controlling and sending data to the NPE. All inputs are sampled on the falling edge of CLK (MC0), pin 37.

Crystal oscillator Y700 drives the CLK input, pin 32, with an 8 MHz signal. This clock signal synchronizes internal operations of the 8 MHz NPE. Jumper J600 provides a way to stop all NPE activities by removing its clock signal for a board test.

The other inputs S0(L), pin 2, and S1(L), pin 1, and COD/INTA, pin 3, provide the NPE with current bus-cycle information.

The input Hold Acknowledge, HLDA (pin 38), line is normally low, to indicate that the EXP controls the buses. When the optional DMA Controller (option 4D) is installed, HLDA tells the NPE, and other devices, that the EXP is not in control of the buses.

Figure X.3. Numeric Processor Interface Timing.

Bus Controller (diagram 23)

Bus Controller U750 provides command and control signals for the Microprocessor and the Executive buses. It decodes EXP status and control lines to generate its command and control signals. Bus Controller outputs are always enabled. U750 produces optimal bus cycle timing (minimum number of CLK cycles per bus cycle) and inserts wait cycles only while the READY(L) input remains high past the fourth CLK cycle. The timing of all bus signals is referenced to the input signal, CLK (MC0). At the falling edge of CLK, the input signals are sampled and the appropriate output signals are asserted.

Bus cycles are started by input signals, S0(L) (MC2) and S1(L) (MC3). Together with M/IO (MC4), they identify the type of bus cycle that is beginning. Table X.3 shows this relationship and the resultant command output.

TABLE X.3
Bus Cycle Type

M/IO	S1(L)	S0(L)	Type of Bus Cycle	Command Output
0	0	0	Interrupt Ack.	INTA(L)
0	0	1	I/O Read	IORC(L)
0	1	0	I/O Write	IOWC(L)
1	0	0	Halt or Shutdown	None
1	0	1	Memory Read (or Inst Read)	MRDC(L)
1	1	0	Memory Write	MWTC(L)

Bus cycles end when the input, READY(L), goes low. Another active or idle bus cycle can begin immediately.

The DT/R (MC13) output signals that the EXP will either transmit or receive data. DT/R is used to control the drive direction of the Data Buffers and is available on the Executive Bus from the Control Buffers U751, U760. The DEN (MC12) output, which is available on the Executive Control Bus, enables the Data Buffers at both ends of the Executive Bus. During consecutive write cycles, DEN remains active and DT/R remains high. If DT/R changes during a bus cycle (see Fig. X.4) it does so when DEN is low so that no more than one device will be driving the data bus at once.

Memory and I/O cycles have the same timing, although a different command output signal is asserted when reading or writing. These command signals are represented by CMD in Figure X.4.

During an Interrupt Acknowledge Cycle (decoded from S0, S1, M/IO), the INTA (MC10) output toggles twice. ALE and MCE (Master Cascade Enable) go high just before each INTA pulse.

MCE enables the Interrupt CAS Address Buffer. This allows the Cascade Address (generated by the Master Interrupt Controller) to be put on the Microprocessor Bus and Executive Bus.

Figure X.4. Bus Controller Read and Write Cycle Timing.

Reset Generator (diagram 23)

The Reset Generator U140 provides a positive power-up reset for the Main Processor Board and the entire instrument. U140's output, pin 5, is gated with CLK (MC0), in the Clock Generator and broadcast as RESET (MC17). In addition to generating a power-up reset, the Clock Generator, U850, also produces a reset if the +5 volt power supply fails.

The power-up reset remains asserted for 60 ms after the +5 volt supply is stable to satisfy the reset timing requirements of the EXP and its coprocessors. The 60 msec delay is set by the 4.7 µF capacitor on pin 3 of U140.

The PWR-UP signal (generated by the power supplies to indicate proper operation) is connected to Resin, pin 2. If PWR-UP goes low due to a power supply problem, a Reset cycle will start. The .1 µF capacitor, C140, on pin 1 of U140 prevents transients on the +5 volt supply from causing spurious resets.

Clock Generator (diagram 23)

The Clock Generator circuit supplies the main clock signal, CLK (MC0), which synchronizes the Executive boards (i.e., those plugged in the Mother board). It also generates the synchronized READY(L) (MC16) and RESET (MC17) control signals. The Clock Generator is comprised of the clock chip, U850, and an inverter, U550E.

The 12 MHz frequency of CLK is derived from crystal oscillator Y950 (U850, pins 7, 8). PCLK (MC1), pin 13, is one half the frequency of CLK and is synchronized with the microprocessor's internal EXP clock. Both CLK and PCLK have a 50% duty cycle.

The READY(L) (MC16) control line informs on-board chips that the current bus cycle is ending. READY(L) is asserted when the SRDY(L) input, pin 2, goes low. U550E inverts the SRDY line for the active low SRDY(L) input. The Executive bus signal, SRDY, is asserted when no additional wait states are needed by peripheral devices (e.g., memory chips, SDI chip, etc). SRDY is a Wire OR signal and is pulled high by a 300Ω resistor connected to +5 volts. This ensures that no wait states are inserted in the EXP bus cycle unless they are requested. Jumper J660 can be used to isolate the EXP from any wait state requests during troubleshooting.

The RESET (MC17) control signal initializes the

- Central Processign Unit (EXP),
- Numeric Processor Extension,
- Bank Decode/Select,
- DMA Controller,
- Diagnostic Status Latch,
- Prevents NV RAM from being written

and, after buffering, also initializes the other Executive Bus boards. Note that the Interrupt Controllers are not initialized by RESET (INIT by Power On or Software). RESET is a clock-synchronized version of the pin 11 input, RES(L).

For the timing of these signals, see Figure X.1, MPB Control Signal Timing under the heading Central Processing Unit (EXP).

Interrupt Address Buffer (diagram 23)

The Interrupt Address Buffer provides the means to coordinate interrupt controllers on other boards with the Interrupt Controllers on the MPB. Half of eight-bit buffer U530B drives the addres lines MA1, MA2 and MA3 with the information on CAS0, CAS1 and CAS2, respectively. The Cascade Address (CAS) lines originate at the Master Interrupt Controller. The Master Cascade Enable, MCE, signal from the Bus Controller is inverted by U550A, then used to enable the Interrupt Address Buffer. J550 can disable this buffer.

Address Decode/Select (diagram 23)

Many VLSI chips on the MPB have a variety of operating modes and must be configured by the EXP to function in the desired mode. Whether initialized at power-up or reprogrammed while running, the devices must first be selected (enabled to receive configuration data), then sent specific commands or data. Device selection is done with the Address Decode/Select circuit, which is mainly composed of U710 and U711 (custom PALs) and U630 (dual 4-input nand gates).

The EXP sends command data to an I/O or memory address reserved for the device being configured (like sending a letter to a mailbox address). The Address Decode/Select circuit decodes the address and control lines and asserts the appropriate chip-select line. The select lines are latched by the Select Latches, then connected to their respective devices. Table X.4 lists the select lines, their associated devices, and their reserved I/O or memory addresses.

TABLE X.4
Select Lines Address Assignments

Select Line	Address Space	Address (In Hex)	Device
S1(L)	I/O	0FBH - 0FEH	Numeric Processor Extension (U400)
S2(L)	I/O	200H - 202H	Interrupt Controller Slave 1 (U321)
S3(L)	I/O	400H - 402H	Interrupt Controller Slave 3 (U340)
S4(L)	I/O	900H - 902H	Interrupt Controller Master (U330)
S5(L)	I/O	0A00H - 0AFFH	DMA Controller (optional) U401)
S6(L)	M	30000H - 33FFFH	Non-Volatile Ram (U200, U210)
S7(L)	M	0F8000H - 0FFFFFH	EPROM (U211, U220)
S8(L)	I/O	8002H	Diagnostic Status Latch (U102A)
S9(L)	I/O	8004H	Wait State Diagnostic Enable (U100D)
S10(L)	I/O	0000H	Memory Bank Select (U550, U530A)

Bank Decode/Select (diagram 23)

To be completed when the circuit is revised.

Data Buffers (diagram 23)

The Data Buffers interface the Microprocessor Data Bus and the Executive Data Bus. They transmit data to or receive data from the Executive Data Bus as directed by the EXP or optional DMA Controller. The Data Buffers connect to the Executive Data Bus with P104.

Data Buffers U860 and U861 are eight-bit bidirectional buffers with tri-state (third state is high impedance) outputs. When disabled their output drivers are set to the high impedance state. This isolation from the Executive bus is necessary for on-board component communication.

The chip enable inputs, pin 19, are connected to the output of the Data Buffer Enable circuit, U740, through jumper J960. Pull-up resistor R960 ensures that the Data Buffers are disabled when J960 is removed.

The drive direction of the Data Buffers is controlled by DT/R (MC13), which is connected to pin 1. When MC13 is high, data is driven to the Executive Data Bus; when low, data is received from the Executive Data Bus.

Address Buffers (diagram 23)

The Address Buffers drive the Executive Address Bus with the address for the current bus cycle. The address can be generated by the EXP or by the optional DMA Controller. In the normal running mode, these buffers are always enabled to drive the Executive Address Bus, at P104.

The eight-bit bidirectional Address Buffers are U650, U651, and U660. Each chip enable, pin 19, is grounded to constantly enable the buffers. Each buffer's direction control (pin 1) is connected to a 4.7 K pull-up resistor and to jumper J800, pin 4. J800 allows the Microprocessor Address Bus to be driven by the Executive Address Bus when diagnostic tests are running. J800 is the Kernal Test connector and is discussed fully in the Diagnostics section of this manual.

Control Buffers (diagram 23)

The Control Buffers provide an interface to the Executive Control Bus for the 16 Microprocessor Control Bus signals, MC0 - MC15. U751 and U760 are eight-line buffers. Their output enables, pins 1 and 19, are grounded to constantly enable the outputs. The buffer outputs connect to the Executive Control Bus with P104.

Data Buffer Enable (diagram 23)

When communication between on-board components is in progress, the Data Buffer Enable circuit disables the Data Buffers. When communication is with the Executive Bus, the data buffers are enabled by DEN (MC12). DEN is generated by the Bus Controller to indicate data is ready to be sent or received.

If any of U740's inputs go low, its output goes high, disabling the Data Buffers. The inputs consist of five Latched Chip Select lines, one control line (DEN(, and ICEN(L)) (equivalent to a

Chip Select), and two lines pulled high with a 4.7 K resistor connected to 5 volts. The Latched Chip Select inputs are:

- LSI Numeric Processor Select
- LS5 Direct Memory Access (DMA) Select
- LS6 Non-Volatile RAM Select
- LLS7 EPROM Select
- LLS10(L) Bank Select

The ICEN(L) input signal is asserted by the Interrupt Controller circuit whenever written or read or an Interrupt Acknowledge Cycle is in progress. During an Interrupt Acknowledge Cycle the Master Interrupt Controller puts a vector address for an interrupt routine on the lower eight lines of the Microprocessor Data Bus which are read by the EXP.

The U740 output (pin 8) goes through jumper J960 before reaching the Data Buffers. Jumper J960 allows the Microprocessor Data Bus to be isolated from the Executive Data Bus while troubleshooting and while running Diagnostics.

Address and Select Latches (diagram 24)

The eight-bit latches U610, U620, U640 and U730 latch and hold the current state of device select lines, S1(L) - S10(L), and address lines, MA1 - MA16, when ALE (MC11) or EALE (Early ALE, U340-6) goes low. The outputs, Latched Address Bus and Latched Select Bus, remain stable until an input changes and another EALE occurs.

Memory Read/Write Control (diagram 24)

The Memory Read/Write Control provides separate write signals for the High and Low bytes of the Non-Volatile Ram. The EXP can read or write on the upper eight data lines, MD8 - MD15, the lower eight data lines, MD0 - MD7, or on all 16 lines at once. The EXP uses status line Bus High Enable, BHE(L), and address line, MA0, to signal which type of data transfer is planned. The Non-Volatile Ram is selected for reading or writing when LS6(L) is asserted. Table X.5 shows the relationships between the state of BHE(L) asnd MA0, the type of data transfer and the enable lines asserted.

TABLE X.5
Enable Scheme for Non-Volatile Ram

Transfer Type	BHE(L)	MA0(L)	Enable Lines
High Byte	0	1	WEH(L)
Low Byte	1	0	WEL(L)
16 Bit Word	0	0	WEH(L), WEL(L)

U110A uses ALE (MC11) to latch BHE(L) (MC14) and MA0. Gate U120A ANDs latched inverted BHE(L), inverted MWTC(L), and inverted Latched Select line LS6(L) to produce the high-byte enable. For the low-byte enable, U120B ANDs latched inverted MA0, inverted MWTC(L), and inverted LS6(L).

Power Down (diagram 24)

The Power Down circuit disables the Non-Volatile Ram when it detects the power supplies failing or an active MRESET signal, or PWR UP false. When the Power Supplies are good, PWR UP is high, and MRESET is low, a one second time delay starts, after which the NV RAM is enabled. The RC time of C151-R164 sets the one second delay.

If PWR UP is pulled low by the power supply logic (R152 is PULL UP), Q170 will turn on which turns off Q171. This causes a low on the chip select line for the Non-Volatile Ram, disabling the RAM.

RAM Battery (diagram 24)

The Ram Battery circuit provides the Non-Volatile Ram (actually they are static rams) with a constant power source if the +5.5 volt power drops ≈+3 volts. The circuit acts as a switch that connects the 3 volt lithium battery BT160 to the VCC inputs, pin 28. The switch also prevents the lithium battery from being charged by the +5.5 volt supply.

CAUTION

Recharging or improper handling of a lithium battery is dangerous. Refer to section 3, Maintenance, of the Volume I Service Manual for proper handling procedures for lithium batteries.

Non-Volatile RAM (diagram 24)

Static ram chips, U260 and U270, are used for permanent storage of high-byte and low-byte data, respectively. The Non-Volatile RAM data lines interface with the Microprocessor Data Bus through the Memory Data Buffers. The chips are enabled for reads or writes by latched RAMSEL(L) (LS6(L)), which can be monitored at TP230. Memory Read/Write Control enables U260 and U270, on pin 27, when data is being written to them. When memory is being read, MRDC(L) (MC6) goes low on pin 22, enabling the output drivers.

The second chip-select input, pin 26, is used to deselect U260 and U270 when the power supplies fail or when the MPB is being reset. This chip enable signal is delayed for one second after a reset or power-up.

The constant VCC power for the static ram chips, which makes them non-volatile, is supplied by the +5.5 volt supply or by a +3 volt battery backup called the Ram Battery. A Ram Battery switching circuit automatically switches the supplies (CR150, CR151).

EPROM (diagram 24)

Part of the operations and diagnostic software resides in two EPROMS (27512s), U240 and U250. They provide 128 K bytes of read-only, permanent memory. The EPROMs are enabled by lached select line LS7(L) on pin 20. The data outputs are enabled by memory read line, MRDC(L) (MC6). The data output lines, which are shared with the Non-Volatile Ram, interface with the Microprocessor Data Bus through the Memory Data Buffers.

The A15 input, pin 1, of the 27512s is conencted to latched address, LA16, by jumper J140. J140 provides for the use of a smaller, alternate EPROM, the 27256.

Memory Data Buffers (diagram 24)

Eight-bit bidirectional buffers U220 and U230 interface the Microprocesor Data Bus to the Non-Volatile Ram and the EPROMs. The Memory Data Buffers allow the Microprocessor Data Bus and the memory devices to meet their timing specifications without causing bus contention.

Removing jumper J330 disables the Memory Data Buffers, which can help isolate problems on the MPB.

Memory Data Buffer Enable (diagram 24)

The three gates of U100 and inverter U510B comprise the Memory Data Buffer Enable circuit. U510B inverts control signal DT/R (MC13) for drive direction control of the Memory Data Buffers. Gate U100A ensures that the Non-Volatile Ram or the EPROM is selected. Gate U100B tests that a memory write, MWTC(L) (MC7), or a memory read, MRDC(L) (MC6), is in progress. Gate U100C checks that the Bus Controller has issued DEN (MC12). When all these conditions are met, the Memory Data Buffers are enabled.

Jumper J330 can be removed to isolate the memories from the Microprocessor Data Bus.

Interrupt Controllers (diagram 24)

The Interrupt Controlelrs constantly monitor the Executive system interrupt lines to ensure that the highest priority interrupt gets serviced first. The Interrupt Controllers provide the ability to assign priority levels to all the system's interrupt lines and to ignore (mask) any of the interrupt lines. Interrupts are service requests for peripheral devices that have data for, or that are requesting data from, the EXP.

The three Interrupt Controllers are programmed by the EXP as the Master, U350, Slave 1, U360, and Slave 3, U370. Their interrupt inputs are programmed for the level-sensing mode. The programming can be done at any time using IORC(L) (MC8), IOWC(L) (MC(9), LA1, and the appropriate Latched Select line. U350 is programmed at I/O address 900-902*hex* (LS4) with the information that it is the Master, input IR1 is Slave 1, and input IR3 is Slave 3. The slaves are programmed at address 200-203*hex* (LS2) and address 400-402*hex* (LS3) for Slaves 1 and 3, respectively. They are told which slave they are so they can respond to the Cascade Address issued by the Master during an Interrupt Acknowledge Cycle.

When a high appears on one of the interrupt request input pins (IR#), the interrupt output INT (pin 17) immediately goes high. If the interrupt was on one of the Master's inputs, its output immediately interrupts the EXP. If the interrupt request was on one of the slaves' inputs, then the slaves' INT output drives the Master and the Master's output drives the EXP. Nothing more happens until the EXP finishes executing its current instruction and is ready to acknowledge ithe interrupt.

To produce an Interrupt Acknowledge Cycle, the EXP drives the M/IO, SO(L), S1(L) and COD/INTA lines low twice, just as it would for two consecutive bus cycles. Each time these lines go low the Bus Controller pulls the INTA(L) (MC10) line low. During the first INTA(L)

pulse, all interrupt requests are latched into the Interrupt Controllers. The Master then decides which of its interrupt inputs has the highest priority, and drives the Cascade Address Bus (CAS0, CAS1, CAS2) with the number for the slave that is attached to that interrupt pin. If the pin is not a slave input, then the Master will drive a zero on the Cascade Address Bus to signal that it will provide the interrupt vector. Through the second INTA(L) pulse the Cascade Address remains valid so the slaves can compare it to their own numbers. If one matches the Cascade Address, it puts a vector number on the Microprocessor Data Bus, which specifies an interrupt handling routine. The timing of these signals, during an Interrupt Acknowledge Cycle, is shown in Figure X.2 under the discussion of the Central Processing Unit (EXP).

A too-short pulse (a glitch) on an interrupt pin will not be latched by the first INTA(L) pulse. When the Interrupt Controller is signaled (by the Cascade Address) to put an interrupt vector number on the data bus, it will erroneously supply the vector number for its lowest priority interrupt. This can cause degraded system performance and possibly corrupted data. (It is good practice not to connect to interrupt IRX7.)

The last chip in the block is U340B, which generates ICEN(L) for the Data Buffer Enable circuit. Each Interrupt Controller has an output called EN(L), pin 16, which it drives low before putting data or a vector number on the data lines. The ICEN(L) signal disables the Data Buffers (U860, U861) when the microprocessor communicates with these interrupt controllers. This eliminates problems with data bus contention when an Interrupt Controllerss are read.

Interrupt Bus Inverters (diagram 24)

The Interrupt Bus Inverters are U561, U570 and U550F. They invert the Executive Bus Interrupt lines, INT0(L) - INT12(L), for the Interrupt Controllers. The input are pulled high by 4.7 K pull-up resistors to ensure that no erroneous interrupts occur when boards are removed from the Executive Bus.

Wait State Generator (diagram 24)

The Wait State Generator (WSG) allows system devices, that need extra time for data transfers, to extend the current bus cycle by 1, 2 or 4 EXP transfer cycles (TC). The inputs to the WSG come from device Select and Latched Select lines and from the I/O board via J77. The output, SRDY, is sampled by the /Clock Generator at the falling edge of phase 1 of the current TC and used to generate the Microprocessor Control Bus signal, READY(L).

A wait state request must be received by D-flip-flop U411B before any wait states will be generated. U720 responds to active select lines with a high output to OR gate U311A. Gate U311A also monitors the I/O Wait Req signal from the I/O board, which signals that a device there is requesting wait states. The output of U311A is the wait request for the D input of U411B. This wait request is clocked in by ALE (MC11). The Q output (pin 9) of U411B is inverted by open-collector U560C to become SRDY. When a wait request is clocked through to set SRDY low, the EXP will insert at least one wait state. The RESET R(L) input, pin 13, will be high at this time.

The remaining WSG circuitry allows the requird number of wait states to be selected. U511 monitors the latched version of the select line inputs. These all require one wait state. U311B has as inputs the I/O one wait request input and the output from U511. Some I/O Board devices require two wait states. The 2 Waits input is buffered by U311C and driven to gate U320B. Four

wait states is the default when a wait request is received and no number of wait states is specified.

Flip-flop U411A and counter U420 count out the requested number of wait states. When the Q output of U411B goes high (because of a wait request), it removes the reset from U441A, pin 1, and from U420, pin 9. With the reset removed, U411A will begin to divide system clock CLK by two. Flip-flop U411A's Q output, pin 5, drives the clock input of the counter, pin 8. At the third rising edge of CLK, the Q1 output (pin 4 of U420) will go high, indicating a completed count for one wait state. If two waits were requested, two clock cycles later U420's Q output, pin 5, will go high. If no number of wait states is indicated, counter U420 will continue counting until its Q4 output, pin 10, goes high. Gate U320C is used to stop SRDY low when one wait state was requested. Gate U320C stop SRDY low when two wait states were required. If the output of either of these gates goes low, or of the inverted four count signal goes low U320A's output (pin 12) will go high. When inverted by U430D this drives the reset input U411B-13 causing the Q output to go low. This signal is inverted and SRDY is driven active, (HI) signaling the end of the wait request. (U411B-13 also resets the wait state generator, U411A and U420.) The asserted SRDY signal is used by the Clock Generator to produce READY(L) (MC16), which signal the end of the current bus cycle.

*No Description of Power On Reset.

Wait State Diagnostic Enable (diagram 24)

The Wait State Diagnostic Enable (WSDE) circuit allows the device ready signal (SRDY) to be monitored on the Executive Bus. An inverted SRDY signal is taken from U411B-9 in the Wait State Generator. SRDY is enabled to the Executive Bus by setting latch output U110B-11 to a high state. When an I/O write (IOWC(L)) occurs and diagnostic select (LS9) is set low, the output of U130D-11 will go low. This low output will be inverted, enabling data bit MD0 to be latched into U110B. If MD0 is high, any change in SRDY will be reflected on the DIAGNSIG(L) line of Executive Bus. If MD0 is low, the SRDY signal will not appear on DIAGNSIG(L).

Diagnostic Status Latch (diagram 24)

The Diagnostic Status Latch latches diagnostic test error codes from the EXP. The latch drives two LEDs and six Error Status Test Points. The error code on MD0 - MD7 will only be lached at the end of an I/O write bus cycle when LS8(L) is active. The reset input, pin 1, ensures that the latched outputs are all low on power-up or after a system reset.

DMA Controller (Optional) (diagram 24)

The Direct Memory Access Controller option, U800, provides high-speed data transfer capabilities for some communications ports. When the DMA is installed, J800 jumper must be moved to pins #1 and #2. (Without the DMA option it goes on.) It is wired in parallel with the Microprocessor Address, Data and Control buses and can use the Executive buses. The DMA Controller requests control of the buses with the HOLD line when one of its DREQ(L) lines is pulled low by a peripheral device and potentially at other times. The EXP grants control with the Hold Acknowledge, HLDA, line. Timing for DMA bus cycles is the same as that of the EXP. For a timing diagram, see the discussion on the Central Processing Unit (EXP). LS5(L), on pin 8, enables the DMA Controller when the EXP is instructing it for its next task.

When the EXP is in the Hold mode, it tri-states all its outputs so that the DMA can drive them. The DMA Controller is programmed through I/O addresses 0A00 - 0AFF*hex*, to let it know where its sequence of instructions is located in memory. The DMA Controller is directed by the EXP to start and to run at a specific maximum number of bus cycles per second. It ha three channels to three different devices. Each channel has a set of DMA Request (DREQ) and DMA Acknowledge (DACK) lines for peripheral-device-initiated transfers. The channel two End of DMA (EOD) line has been programmed as a general all-channel interrupt to the EXP. This is used to tell the EXP that the DMA is finished with its assigned task.

When the DMA Controller is not installed, the EXP handles the peripheral device requests with interrupt service routines.

A18 Memory Board

The Memory Board provides the Executive Processor (EXP) with dynamic RAM and EPROM for most operations. Support circuitry for the memories and diagnostic circuitry for troubleshooting are located on-board. All accesses to DRAM or EPROMs are initiated by the Main Processor Board (MPB) and specifically by the 80286 Executive Processor or the optional DMA Controller. See the discussion of the Main Processor Board in this section for bus cycle timing information.

Test points TP200, TP500 and TP800 provide ground connections for test instrument probes.

Address Latches (diagram 25)

Address Latches U540, U640 and U642 buffer and hold the Executive Address lines and BHE(L) for the EPROMS, DRAM Controller and other on board devices. With their outputs always enabled, these latches act as buffers which allow addresses to pass through as soon as they are available. The addresses are latched when the LE input is driven low by MRDC(L), MWTC(L) or IORC(L) from the MP. At the end of a memory cycle, LE goes high and the latches again act as buffers. LE can be monitored on test point TP801.

Address Decode (diagram 25)

Programmable array of logic (PAL) U542 decodes the address lines to produce RAM select signal RAM SEL(L) and four EPROM bank-select signals, CS1(L) - CS4(L). RAM SEL(L) enables the DRAM Controller to begin a DRAM access cycle. Each EPROM select line is latched, along with four Executive address lines, by U540. The latch outputs are always enabled. While latch enable (LE) is low the latch outputs are responsive to changes on the inputs. Table X.1 shows the addresses that U542 requires to produce the select outputs.

TABLE X.1
PAL Address Decoding

Select	Address Range	Chips Enabled
RAM SEL(L)	0 - 01FFFF, 20000 - 3BFFF (Bank #1)	All RAM
CS1(L)	080000 - 09FFFF	U630, U730
CS2(L)	0A0000 - 0BFFFF	U620, U720
CS3(L)	0C0000 - 0DFFFF	U612, U712
CS4(L)	4C0000 - 4DFFFF	U600, U700

The real address line inputs A14 - A19 are generated by the EXP on the MPB. Lines A20 - A23 and EPON are memory bank-select lines, which are encoded by the Bank Select circuitry on the MPB.

EPROM Select (diagram 25)

The EPROM Select circuitry provides latched EPROM bank-select lines and an enable signal for the EPROM Data Buffers. Transparent latch U540 buffers the EPROM bank-select lines and drives them on its constantly enabled outputs. The outputs reflect changes on the inputs until the latch enable (LE) input goes low, at which time the current inputs are latched onto the outputs. At the end of a memory cycle, LE becomes high causing U540 to become transparent and ready for another memory cycle. The LE signal can be monitored on TP801.

When gate U632A detects an active EPROM bank-enable line, it generates EPROM SEL, which enables the EPROM Data Buffers. EPROM SEL also signals the Memory Wait State Generator to request wait states from the EXP. EPROM SEL can be monitored on test point TP806. Jumper J543 allows the EPROM Data Buffers to be constantly enabled during diagnostic testing. The EPROM bank-select lines can be monitored on one of the test points TP802 - TP805.

EPROM (diagram 25)

The EPROMs contain most of the operating system code and diagnostics code for the EXP. All the EPROMs share the latched address bus (these address lines are just buffered until the middle of the access cycle when they get latched). The EPROMs are organized into high- and low-byte pairs or banks. Each bank is selected by a separate chip-enable signal, which is generated by the Address Decode PAL. The output data drivers of an EPROM bank are enabled when the bank is selected. The high-byte chips share data lines ED8 - ED15 and the low byte chips share data lines ED0 - ED7. These data lines are buffered to the Executive Data Bus by the EPROM Data Buffers.

The EPROMs installed can be either 27256s or 27512s. The circuit is configured by moving jumper J541. The standard instrument is supplied with 27512s. In the standard configuration, J541 should be in the "A" position.

EPROM Data Buffers (diagram 25)

The EPROM Data Buffers drive data from the EPROMs on the Executive Data Bus. Both eight-bit buffers are enabled by the output of U830A when all its inputs are high. The enable line can be monitored on test point TP809. The inputs to U830A are: EPROM SEL, which signals that an EPROM bank is selected; BDEN, which signals that the EXP is ready to read data; and inverted DT/R, which signals whether the memory operation is a read or write.

Bank Enable (diagram 25)

The Bank Enable circuitry buffers address lines A20 - A23 to produce bank-select address lines BA0 - BA3. These lines can be monitored on test points TP501 - TP504, respectively. U530 gates BA0 and BA1 with latched address line LA17 to produce the bank-select signals used by the DRAM Controller.

Memory Wait State Generator (diagram 25)

When a memory access starts, the Memory Wait State Generator signals the EXP to extend the bus cycle a specific number of clock cycles.

When an EPROM bank is selected, the EPROM SEL line goes high at the D input of U820B. If jumper J800 is not set on zero waits, the high will be clocked by S CLK to the Q output. The high Q output is SRDY(L), which is inverted by U552 to drive the system signal SRDY. When SRDY is driven low, it signals the EXP to begin inserting wait states. The high Q output also removes the reset condition from U820A. U820A divides the S CLK signal by two and clocks shift register U810. Jumper J800 determines which output of U810 gets inverted by U732A, and therefore, how long SRDY remains low. When the selected output of U810 goes high, it causes U820B to be reset, along with rest of the EPROM wait circuit, ending the wait request condition. Test point TP808 can be used to monitor SRDY(L), which signals EPROM wait requests. SRDY(L) also can be read by the diagnostics with And gate U452B.

Wait requests from the DRAM Controller, AACKA(L), are ANDed with L RAMSEL, which is latched inverted RAM SEL(L). The output of gate U530A is inverted and used to pull SRDY low, requesting wait states from the EXP. The DRAM Controller determines the number of wait states requested. Test Point TP206 can be used to monitor this line.

Memory Diagnostic Signal Select (diagram 25)

This diagnostic circuit causes either of two signals generated on the board to be driven on the Executive Bus line DIAG SIG(L). One signal is SRDY(L), which is generated by the Memory Wait State Generator. The other is a combination of the DRAM row address strobe lines. Reading either of these signals requires a write to diagnostic I/O address 8020*hex*. The address is decoded and the resultant active low signal is latched into U352A by BALE. The latched output is gated with IOWC(L) (I/O write) by U450D. When this output is high the latch U352B is enabled and data lines D0 and D1 are latched. D0 enables the read of SRDY(L) and D1 enables the read of the combined row address strobes. This last signal can be monitored on test point TP204.

Memory Configuration Readback (diagram 25)

This circuit allows the diagnostics to read the position of the memory configuration jumpers and the Bank enable lines. The Executive Processor does an I/O read at address 8040*hex* to read the information on the lower eight data lines. U350A decodes the address and produces a low signal, which is latched by U352A when BALE goes high. The latched enable signal is gated with IORC(L) (I/O read) and used to enable the read buffer U832.

Dram Controller (diagram 26)

DRAM Controller U410 is configurable for DRAMs of different sizes and speeds in a two- or four-bank arrangement. It provides high speed access to the standard two banks of 64 kilobyte DRAM chips, and it automatically provides refresh signals. Though the DRAM Controller supports dual-port access to the DRAM, this circuit uses only the port A interface. In addition

to the DRAM Controller chip, a set of initialization shift registers and a high/low bank enable circuit are in this block.

The EXP cannot access the DRAM on power-up or on reset until the DRAM Controller has been configured. The DRAM Controller is configured while the rest of the instrument is in its 45 msec reset state. The on-board Reset Generator produces a 10 msec reset pulse when the system reset goes active. During this time, shift registers U320 and U420 are loaded via jumpers J322 and J422 with the configuration data for the DRAM Controller. After 10 msec the reset signal is removed from the DRAM Controller. The DRAM Controller then produces 16 clock pulses from its MUX/PCLK output that shifts the 16 configuration data bits into the PDI input. This takes about 20 µsec. About 30 msec later the rest of the system will come out of reset and the EXP will access the DRAM.

The system status lines S0(L) and S1(L) are inverted and used to drive the RDA(L) and WRA(L) inputs. These signals are generated by the EXP. RAM SEL(L), generated by Address Decode, enables port A of the DRAM Controller at input PEA(L) to allow DRAM accesses.

The BS0 and BS1 inputs select which DRAM bank is to be accessed. Address inputs AL0 - AL8 are used to generate the row address, and inputs AH0 - AH8 are used to generate the column address.

The output AACKA(L) signals the EXP that additional time is needed for a DRAM access. Outputs WE and PSEN are gated by U332B, C and U340B,C with latched inverted versions the EXP signals BHE and A0(L) The gates produce write enable signals HBYTE WE(L) and LBYTE WE(L). BHE and A0(L) are also gated with latched RAM SEL to produce the DRAM Data Buffers enable signals HBYTE OE(L) and LBYTE OE(L). These enable signals can be monitored on test points TP300 - TP303. In addition, latched RAM SEL can be monitored on test point TP205. Figure X.X shows the signal timing for DRAM accesses.

Figure X.X DRAM Access Timing

Also in this circuit block, the EXP transmit and receive signal DT/R is buffered. When the EXP is reading from DRAM, the output enables of the DRAM are activated by BDT/R. Inverted DT/R is used to select the drive direction for the DRAM Data Buffers and can be monitored on test point TP207.

Dram (diagram 26)

In the standard configuration, the DRAM is comprised of two banks of four 64 kilobyte by four bit DRAMs. The Memory Board is designed to allow two more banks to be added later as an option. The two banks used are:

Bank 1 U110, U112, U120 and U122,

Bank 2 U210, U212, U220 and U222.

The DRAM Controller and the buffered EXP control line DT/R control the DRAM. The DRAM may be written to with just a high or low-byte of data. The high and low write-enable lines provide this function. Reading just a high or low byte is controlled by enabling one of the DRAM Data Buffers with the output control lines. Data to and from the DRAM chips uses the RD data

lines, which are paralleled to each bank. The RD data lines are buffered by the DRAM Data Buffers to the Executive Data Bus. Access timing is shown in this section in the DRAM Controller discussion.

Dram Data Buffers (diagram 26)

The DRAM Data Buffers provide an interface between the DRAM data bus and the Executive Data Bus. Drive direction is controlled by the inverted EXP control signal DT/R. Each buffer chip can be enabled separately to allow just high or low byte reads and writes. Signal HBYTE OE(L) enables high-byte buffer U740; likewise, LBYTE OE(L) enables low-byte buffer U742. The in-line resistor packs provide impedance matching between the DRAMs and the buffers.

Dram Configuration (diagram 26)

The DRAM Configuration jumpers allow the DRAM to be arranged in different ways to facilitate various customer options and design considerations. The jumpers select which address and bank-select lines will be applied to the DRAM Controller. Jumper J521 provides for use of 64 K or 256 K bit DRAMs. J501 allows two additional banks of DRAM to be added. J520 provides for switching to the virtual addressing mode of the EXP.

Dram Controller Reset Generator (diagram 26)

The DRAM Controller Reset Generator monitors the system RESET line and uses it to generate a shorter reset pulse for the DRAM Controller. The 45 msec system RESET pulse is buffered, then differentiated. The resultant quick pulse is applied to the input RESIN. U430 produces a 10 msec reset pulse, which appears on the output where it gets inverted and applied to the DRAM Controller. It gets inverted again and applied to the shift and load inputs of shift registers U320 and U420. When power is first applied to the instrument, U430 monitors the +5 volt line. When the +5 V line reaches 4.7 volts, the RESET(L) output is driven active and remains active for 10 msec. After this delay the RESET(L) output is brought back high.

Part 2
Performance Verification Procedure

NOTE

The Performance Verification Procedure is located in the 11401/11402 User's Reference Manual.

Part 3
Adjustment Procedure

Preliminary
Adjustment Procedure

NOTE

This procedure is intended to provide a way to manually set all internal adjustments. Consult the User's Reference manual for more information about advertised specifications and instrument operation. Consult the test equipment manuals for information concerning test equipment setup or interconnection.

A separate procedure is provided in the User's Reference manual to verify basic instrument operation without checking all features and performance requirements.

Introducing the 11401 and 11402 Digitizing Oscilloscopes, an introductory operator's manual, contains step-by-step procedures designed to familiarize the first-time user with instrument features.

Preliminary Information

Using This Procedure

In this procedure, capital letters within the body of text identify front-panel controls, indicators, and connectors (e.g., MEASURE) on the 11401/11402. Bold and italicized letters identify menu labels and display messages. Initial capital letters identify connectors, controls, and indicators (e.g., Position) on associated test equipment. Initial capital letters also identify adjustments inside the 11401/11402 (e.g., Vert Pos).

A heading system is used to readily identify the steps that contain performance check and/or adjustment instructions. For example, if CHECK is the first word in the title of a step, an electrical specification is checked. If ADJUST is the first word in the title, the step contains one or more internal adjustments. If CHECK/ADJUST appears in the title, the step involves electrical specification checks and related adjustments. If EXAMINE is the first word in the step title, the step concerns measurement limits that indicate whether the instrument is operating properly; these limits are not to be interpreted as electrical specifications.

The alphabetical instructions under each step (a, b, c, etc.) may also contain CHECK, EXAMINE, ADJUST, or INTERACTION as the first word of the instruction. These terms are defined as follows:

ADJUST—describes which adjustment to make and the desired result. We recommend that the adjustment not be made if a previous CHECK or EXAMINE instruction indicates that no adjustment is necessary.

CHECK—indicates that the instruction accomplishes an electrical specification check.

EXAMINE—usually precedes an ADJUST instruction and indicates that the instruction determines whether adjustment is necessary. If no ADJUST instruction appears in the same step, the EXAMINE instruction concerns measurement limits that have no related adjustment. Measurement limits following the word EXAMINE are not to be interpreted as specifications.

They are provided as indicators of a properly functioning instrument and to aid in the adjustment process.

INTERACTION—indicates that the adjustment described in the preceding instruction interacts with other circuits. The nature of the interaction is described and reference is made to the step(s) affected.

Power-Up Defaults

At the initial power-up, the 11401/11402 assigns default front-panel settings and operating parameters. In this procedure, those default settings are used unless a change is specifically indicated. Changing any default setting other than those indicated may cause erroneous or unexpected results.

Menu Selections

Although brief instructions are included in the procedure for making menu selections, detailed descriptions of those menus as well as instructions on how to exit menus after selections are made are generally not included. Comprehensive descriptions of menus and instrument features are found in the User's Reference Manual.

Vertical and Horizontal Settings

Selection of vertical and horizontal settings for the 11401/11402 is done via two touch-panel icons, Vertical Size and Position and Horizontal Size and Position. These icons assign the function of the two front-panel control knobs. One or the other icon will be highlighted, which determines whether the Top and Bottom Control knobs are assigned to vertical or horizontal settings. Display labels to the left of the knobs indicate their current assignment. Knob assignments may be changed to the other axis by simply touching the dimmer of the two icons. Knob sensitivity may be changed with menus accessed by touching the knob labels.

In this procedure, instructions are not provided for selecting the required vertical and horizontal settings. Detailed instructions for operating the 11401/11402 display are given in the User's Reference manual. Familiarity with these operating principles is essential to perform the Adjustment and Performance Check procedure.

Plug-in Unit Installation and Removal

The front-panel ON/STANDBY switch should be set to STANDBY before installing or removing plug-in units. After the plug-in unit is installed, the switch may be set back to ON. The instrument will first perform its normal diagnostic and self-test sequence, then restore the front-panel settings in effect at the time of the power-down.

Required Test Equipment

The following equipment is required for the adjustment and performance check procedure.

1. **Signal Standardizer.** Tektronix 067-0587-02 Signal Standardizer Calibration Fixture with the interface connector modified for 11000-series use.

2. **Test Oscilloscope.** Tektronix SC 504 80 MHz Oscilloscope. (NOTE: Step D5 requires an oscilloscope having a bandwidth of ≥150 MHz.)

3. **Probe.** Tektronix P6102A. (NOTE: Step D5 requires a probe capacitance of ≤12 pF.)

4. **Probe-Tip Ground Adapter.** Tektronix Part 013-0085-00 Bayonet Ground Assembly

5. **Digital Voltmeter.** Fluke 8842A digital voltmeter.

6. **Frequency Counter.** Tektronix DC 503A Universal Counter/Timer with a TM 5000-Series Power Module

7. **Test Terminal.** Compaq Portable II PC with ProComm software. The test terminal may be any GPIB (IEEE-1978) controller, or ASCII terminal equipped with an RS-232-C port.

8. **Term Conn Link (shorting strap).** Tektronix Part 131-0993-00.

9. **Alignment Tool (plastic hex).** Tektronix Part 003-0301-00.

10. **Alignment Tool (insulated slot).** Tektronix Part 003-0675-01.

11. **Alignment Tool (square-tip).** Tektronix Part 003-1400-00.

12. **Magnetic Screwdriver.** Tektronix Part 003-0293-00.

13. **Torx screwdriver tips:**
    #10 . . . Tektronix Part 003-0814-00
    #15 . . . Tektronix Part 003-0966-00
    #20 . . . Tektronix Part 003-0866-00

Adjustment Procedure Index

Power-Up Sequence

1. Remove the top and bottom covers from the 11401/11402.

2. Connect the 11401/11402 to a suitable power source and switch the rear-panel PRINCIPAL POWER SWITCH to ON.

3. Switch the front-panel ON/STANDBY switch to ON.

4. Allow the 11401/11402 to warm-up for at least 20 minutes.

5. Press the 11401/11402 ENHANCED ACCURACY button.

A. Power Supply

A1. +5.2 V Reference (A3R800)

NOTE

The +5.2 V Reference adjustment is set at the factory using special test fixtures, and should not need readjustment. If readjustment does become necessary, refer to your local Tektronix Service Center or Field Representative.

A2. Adjust Regulator Reference (A4R830)

NOTE

The +10 V Ref adjustment is set at the factory using special test fixtures, and should not need readjustment. However, if circuit boards have been replaced, or if R830 has been replaced, the following procedure will allow you to set the reference voltage to allow nominal instrument operation.

Unless otherwise stated, all 11401/11402 settings are power-up default.

SETUP CONDITIONS

No plug-ins installed.
Connect the negative lead of a Digital Voltmeter to the COM Test Point on the A4 Regulator Board.
Connect the positive lead to the REF Test Point on the A4 Regulator board. (refer to Figure A at the end of this procedure.)

Settings:

11401/11402
No change.
Digital Voltmeter
Mode.....DC Voltage

a. **ADJUST—+10 V Ref adjustment R830 on the A4 Regulator board for +10.000 volts.**

B. Display

B1. Preliminary Setup Conditions

Remove 2 screws in CRT protector shield and remove shield.

B2. Adjust Crt Driver (A8R202, A8R520, A8R530, A8R620, A8L120, A8R541, A8R621, A8R540, A8R100)

WARNING

Shock hazard exists while CRT protective shield is removed.

NOTE

Unless otherwise stated, all 11401/11402 settings are power-up default.

SETUP CONDITIONS

No plug-ins or test equipment required.
Refer to Figure A at the end of this procedure.

a. **ADJUST**—Main Brite adjustment R202 clockwise until the raster appears.

b. **ADJUST**—Horiz Hold adjustment R620 and Vert Hold adjustment R530 for a stable display on the screen.

c. Press the 11401/11402 UTILITY menu button.

d. Select **Extended Diagnostics** in the menu/status area, **Front Panel** from the Block menu appearing in the display area, and **Area** from the menu/status area.

e. Select **Verify** from the Area menu, **Routine** from the menu/status area, and **Softkeys** from the Routine menu.

f. Select **Run** from the menu/status area. A grid pattern will fill the display area.

g. ADJUST—Vert Hold adjustment R530 so the bottom line is at or near the bottom of the raster.

h. ADJUST—Vert Pos adjustment R520 and Vert Size adjustment L120 to align the grid with the index bumps along the inside vertical edge of the front-panel bezel. There are three indexes along each side: one near each corner and one in the center. Looking straight into the CRT to eliminate any parallax error, align the top of the grid display with the top vertical index, the bottom of the grid with the bottom index, and the grid center line with the center index. Optimize the settings of R520 and L120 for best overall alignment.

i. ADJUST—Horiz Lin adjustment R541, Horiz Size adjustment R621, and Horiz Pos adjustment R540 for best overall linearity and position. Use the horizontal indexes along the top and bottom of the front-panel bezel to align the grid by the same method used for the vertical adjustments.

j. INTERACTION—R621 Horiz Size, R541 Horiz Lin, and R540 Horiz Pos interact and may need readjustment.

k. Touch the **Exit (E)** label in the grid display then the **(E) Exit** label in the menu/status area.

l. ADJUST—Main Brite adjustment R202 counterclockwise until the retrace lines are just extinguished.

m. Select **Instr Options** from the menu/status area and **Display Intensity** from the **Instr Option** menu.

n. Use either control knob to set the display intensity to 100%.

o. ADJUST—Focus adjustment R100 for best overall focus.

p. Set control knob for normal intensity.

q. Replace crt protective shield.

C. Input/Output

C1. Preliminary Setup Conditions

a. Set the 11401/11402 front-panel ON/STANDBY switch to STANDBY.

b. Remove L bracket on front of card cage. Remove both plastic retaining strips on top of card cage. Remove the A17 Main Processor board and place it in the fourth slot. Remove A14 I/O board and place in 3rd slot. Move the A18 Memory board from the first slot to the fifth slot. Reconnect cable to A14 I/O board.

c. Set the 11401/11402 front-panel ON/STANDBY switch to ON.

C2. Examine/Adjust Real Time Clock (A14C510)

NOTE

Unless otherwise stated, all 11401/11402 settings are power-up default.

SETUP CONDITIONS

Connect the Frequency Counter to TP310 on the A14 Input/Output board. (Refer to Figure B at the end of this procedure.)

Settings:

11401/11402
No changes.
Counter
Mode.....Period
Trigger.....DC
Slope.....–
Time Base.....1 MHz

a. Press the 11401/11402 UTILITY menu button.

b. Select **Extended Diagnostics** from the menu/status area and **Internal I/O** from the Block menu.

c. Select **Realtime Clk** from the Area menu and **Calibrate** from the Routine menu.

d. Select **Run**.

e. CHECK—for a period of 1,000,000 µs (1 s) , within the limits of 1,000,050 µs and 999,995 µs.

f. ADJUST—Real Time Clock adjustment C510 for 1,000,000 µs.

C3. Examine/Adjust +6.5 V Reference (A14R112)

NOTE

Unless otherwise stated, all 11401/11402 settings are power-up default.

SETUP CONDITIONS

Connect a Digital Voltmeter to TP114 and GND (TP102) on the A14 Input/Output board. (Refer to Figure B at the end of this procedure.)

Settings:

11401/11402
No change
Digital Voltmeter
Mode.....DC Voltage

a. **CHECK**—for +6.500 V, within the limits of +6.505 V and +6.495 V.

b. **ADJUST**—+6.5 V adjustment R112 for +6.500 V.

C4. Examine/Adjust Temperature Sensor (A14R110)

NOTE

Unless otherwise stated, all 11401/11402 settings are power-up default.

SETUP CONDITIONS

Connect the Digital Voltmeter to pin 3 of U124 and GND (TP102) on the A14 Input/Output board. (Refer to Figure B at the end of this procedure.)

Settings:

No change

a. **CHECK**—for +2.455 V, within the limits of +2.450 V and +2.460 V.

b. **ADJUST**—Temperature Sensor adjustment R110 for +2.455 V.

c. Set the 11401/11402 front-panel ON/STANDBY switch to STANDBY.

d. Move all boards back to their original location.

e. Set the 11401/11402 front-panel ON/STANDBY switch to ON.

NOTE

Make certain to re-enter Enhanced Accuracy mode after 20 minutes has elapsed.

D. Acquisition

D1. Adjust 10 MHz Signal Amplitude (A5C217)

NOTE

Unless otherwise stated, all 11401/11402 settings are power-up default.

SETUP CONDITIONS

Turn instrument on its left side to expose the bottom. Remove the eight screws securing the A5 Acquisition board (located on the bottom of the instrument). Swing board out on hinges and lock in place. Connect the Test Oscilloscope to TP214 on the A5 Acquisition board. (Refer to Figure B at the end of this procedure.)

Settings:

11401/11402
    No change
Test Oscilloscope
    Vertical.....500 mV/division
    Horizontal.....50 ns/division
    Triggering.....Internal

a. **ADJUST**—10 MHz adjustment C217 for maximum signal amplitude (typically about 1.4 v p-p).

D2. Examine/Adjust Phase Lock Loop (A5C500)

NOTE

Unless otherwise stated, all 11401/11402 settings are power-up default.

SETUP CONDITIONS

Connect a Digital Voltmeter to TP410 on the A5 Acquisition board and chassis ground. (Refer to Figure B at the end of this procedure.)

Settings:

No change

a. **CHECK**—for +6.0 V, within the limits of 6.3 V and 5.7 V.

b. **ADJUST**—VCO adjustment C500 for 6.0 V.

D3. Examine/Adjust Differential Amplifier V+ (A5R666)

NOTE

Unless otherwise stated, all 11401/11402 settings are power-up default.

SETUP CONDITIONS

Connect the test leads of a Digital Voltmeter to TP660 and TP665 on the A5 Acquisition board (disregard polarity). (Refer to Figure B at the end of this procedure.)

Settings:

No change.

a. **EXAMINE**—the voltmeter for 10.500 V, within the limits of 10.510 V and 10.490 V.

b. **ADJUST**—Diff Amp V+ adjustment R666 for 10.500 V.

D4. Examine/Adjust Calibration System Voltage Reference (A5R1576, A5R1582)

NOTE

Unless otherwise stated, all 11401/11402 settings are power-up default.

SETUP CONDITIONS

Connect the positive lead of the Digital Voltmeter to the front-panel CALIBRATOR probe connector. Connect the negative lead to the front-panel ground post.

Settings:

No change

a. Press the 11401/11402 UTILITY menu button.

b. Select **Extended Diagnostics** from the menu/status area and **Points Acq** from the **Block** menu.

c. Select **Cal Refs** from the **Area** menu and **FP –10.00 V** from the **Routine** menu, and **(r)Run** in the menu/status area.

d. EXAMINE—the Voltmeter for –10.000 V within the limits of –10.002 V and –9.998 V.

e. ADJUST—Offset adjustment R1576 on the A5 Acquisition board for –10.000 V.

f. Select the **Exit (E)** label.

g. Select **FP –9.9951 V** from the **Routine** menu, and **(r)Run** in the menu/status area.

h. EXAMINE—the Voltmeter for +9.995 V, within the limits of +9.993 V and +9.997 V.

i. ADJUST—Gain adjustment R1582 on the A5 Acquisition board for +9.995 V within the limits of +9.993 V and +9.997 V.

j. Select the **Exit** label.

D5. Examine/Adjust Difference Amplifier Step Response (A5C253)

NOTE

Unless otherwise stated, all 11401/11402 settings are power-up default.

SETUP CONDITIONS

Set the ON/STANDBY switch to STANDBY.
Install a Signal Standardizer in the left plug-in compartment.
Set the ON/STANDBY switch to ON.
Attach a probe-tip ground adapter to the test oscilloscope probe.
Refer to Figure B at the end of this procedure for adjustment locations.

Settings:

11401/11402
Waveform Menu
Vertical Description.....Left
Signal Standardizer
Test.....Vert or Horiz +Step Resp
Rep Rate.....1 MHz
Test Oscilloscope (refer to required test equipment at the start of this procedure)
Vertical.....200 mV/div, DC
Horizontal.....20 ns/division
Triggering.....DC, +, Normal

a. Set the Signal Standardizer Amplitude control fully clockwise (10 div. display). Position the top of the square wave to the center horizontal graticule line on the 11401/11402 display graticule.

b. Connect the Test Oscilloscope to R650 (U552 end), on the A5 Acquisition board.

c. Connect the ground contact of the probe-tip ground adapter to a near-by ground point, such as pin 4 of R451.

d. Set the Test Oscilloscope center horizontal graticule line to 0 volt.

e. Set the Test Oscilloscope Trigger Level to the maximum positive level, then slowly lower it until triggering occurs on the most positive spike (refer to Fig. 1B).

NOTE

If the waveform envelope is not visible on the Test Oscilloscope display as shown in Figure 1, slowly rotate the Signal Standardizer Position control until the envelope appears. If the envelope is not equally positioned around the 0 V point, press the 11401/11402 ENHANCED ACCURACY button. The envelope is actually the step response waveform of Difference Amplifier U443 and is the portion that will be adjusted in the following steps.

f. **EXAMINE**—The Difference Amplifier waveform for optimum adjustment as shown in Figure 1(C).

g. **ADJUST**—Diff Amp Comp adjustment C253 (using the square-tip alignment tool) for the fastest rise time with minimum overshoot. Note that C253 adjusts both the + and – steps and they become optimum at different settings. Compromise the adjustment for best + and – step response. Figure 1(C) shows optimum adjustment.

h. Reposition the A5 Acquisition board and secure with the eight screws removed earlier.

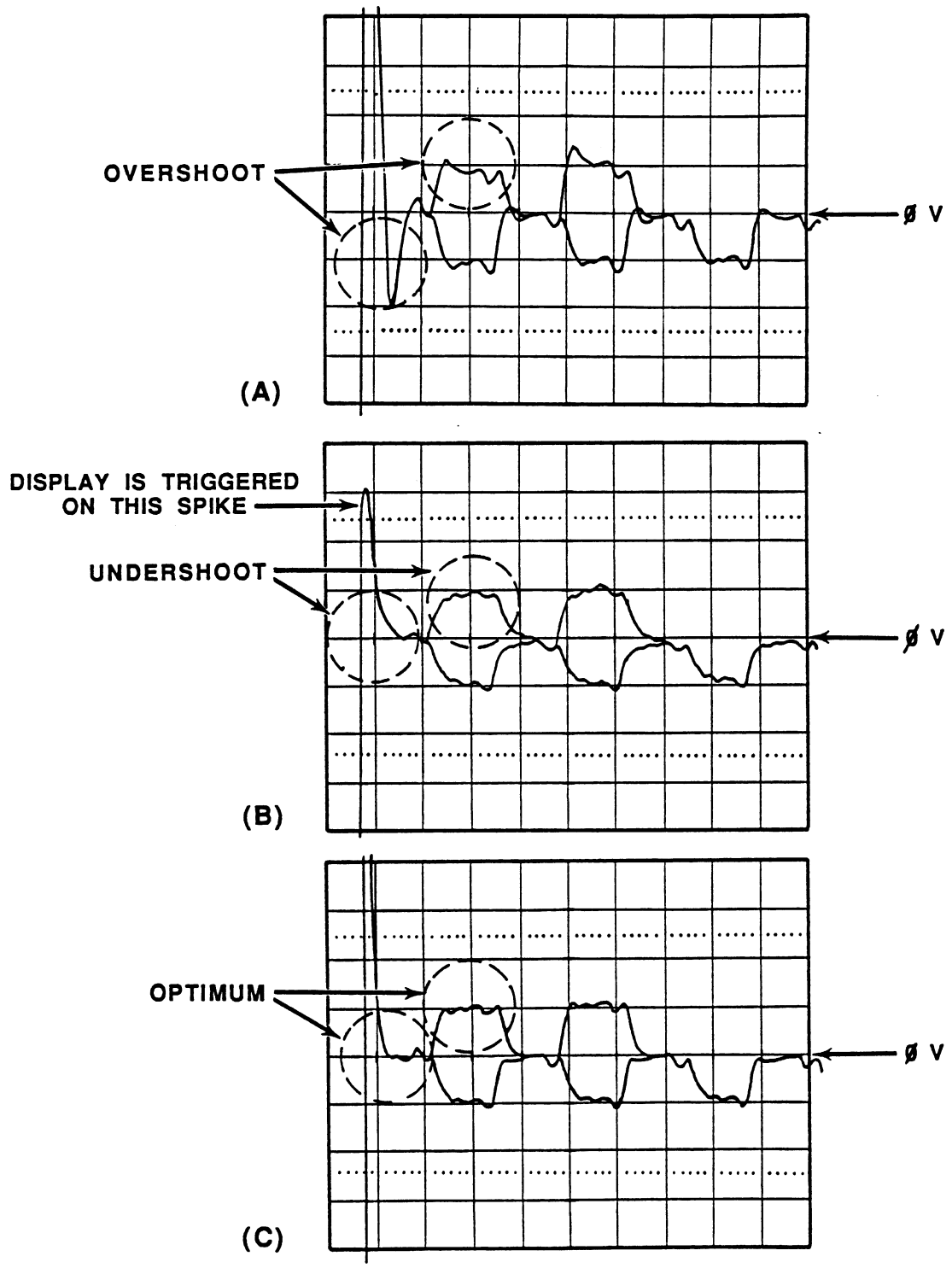


Figure 1. Difference Amplifier Waveform displays.

E. Sampler and Digitizer

E1. Set Sampler Gain

NOTE

Unless otherwise stated, all 11401/11402 settings are power-up default.

SETUP CONDITIONS

Install the Signal Standardizer in the left plug-in compartment.
Connect the Test Terminal to the 11401/11402 rear-panel RS-232-C connector.
Install a Term Conn Link (shorting strap) on the CAL-LOCK terminals located on the bottom of the A6 Time Base board. (see Fig. C at the end of this procedure for location).

Settings:

11401/11402
Waveform Menu
- Vertical Description ..... **Left**
- Trigger Menu ..... **Auto**

Top Control Knob (Horizontal) **Main Size** ..... 10 ms/div
Measure menu ..... **Peak to Peak**
Utility menu
- **RS232C Parameters**
- **Echo** ..... **On**
- **Verbose** ..... **On**
- **Baud Rate** ..... **9600 Bd** (depends on Test Terminal)

Signal Standardizer
- Test ..... Vert or Horiz Gain
- Rate ..... 1 kHz
- Position ..... Center display on screen

a. Enter a temporary Cal Constant value of 9700 into NV RAM as follows:

- Type `mcalconst 134:9700` on the Test Terminal keyboard.
- Press RETURN button.
- Test terminal should respond "OK".
- Press ENHANCED ACCURACY button on 11401/11402 front panel. Allow about one minute for the instrument to complete the Enhanced Accuracy Routine, as indicated by a message on the screen.

b. Press the MEASURE button on the 11401/11402 front panel. Note the measured peak to peak amplitude from the menu/status area (e.g., 9.370 V).

c. Repeat part b. for the Center and Right plug-in compartments as follows:

CAUTION

To prevent possible instrument damage, you must set the ON/STANDBY switch to STANDBY before removing or inserting plug-in units.

NOTE

*After each power-up in this step you must wait about one minute for the instrument to complete the Enhanced Accuracy routine, as indicated by the message "**Warmup Complete. Enhanced Accuracy In effect**" displayed at the top of the screen.*

Note the amplitude measurement for the Center and Right plug-in compartments by installing the Signal Standardizer in each, selecting that compartment for display and reading the peak-to-peak measurement value from the display menu/status area.

d. Calculate the median amplitude gain from the three peak-to-peak voltage readings noted above, as follows:

$$\text{Median Amplitude} = \frac{\text{Min} + \text{Max}}{2}$$

where:

Min = the lowest of the three measured peak-to-peak signal amplitudes (in volts).

Max = the highest of the three measured peak-to-peak signal amplitudes (in volts).

EXAMPLE:

The three measured gain values are 9.38, 9.37, and 9.33.

$$\text{Median Amplitude} = \frac{9.38 + 9.33}{2} = 9.355\ \text{V}$$

e. Calculate the Cal Constant that will be used to set the sampler gain as follows:

$$\text{Cal Constant} = \frac{\text{Median Amplitude}}{10} \times \text{Temporary Cal Constant}$$

EXAMPLE:

$$\text{Cal Constant} = \frac{9.335}{10} \times 9700 = 9074$$

f. Set the 11401/11402 sampler gain by entering the result of the Cal Constant (9074) calculation back into the sampler with the Terminal Cal Constant command as follows:

- Type `mcalconst 134:9074` on the Test Terminal keyboard.
- Press RETURN button.
- Test Terminal crt display should respond "OK".
- Press ENHANCED ACCURACY button on 11401/11402 front panel.

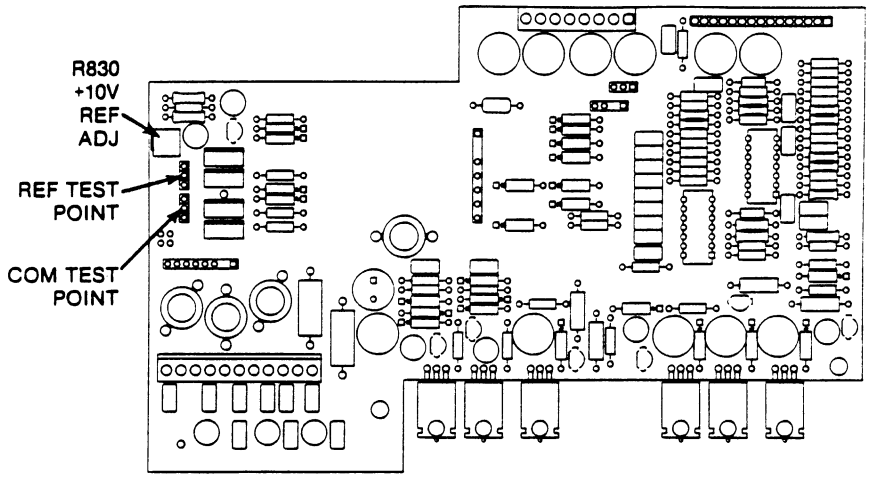
g. To ensure that the new cal constant has been incorporated in nonvolatile RAM:

- Type `mcalconst? 134` on the test terminal.
- The Test Terminal crt display will respond:

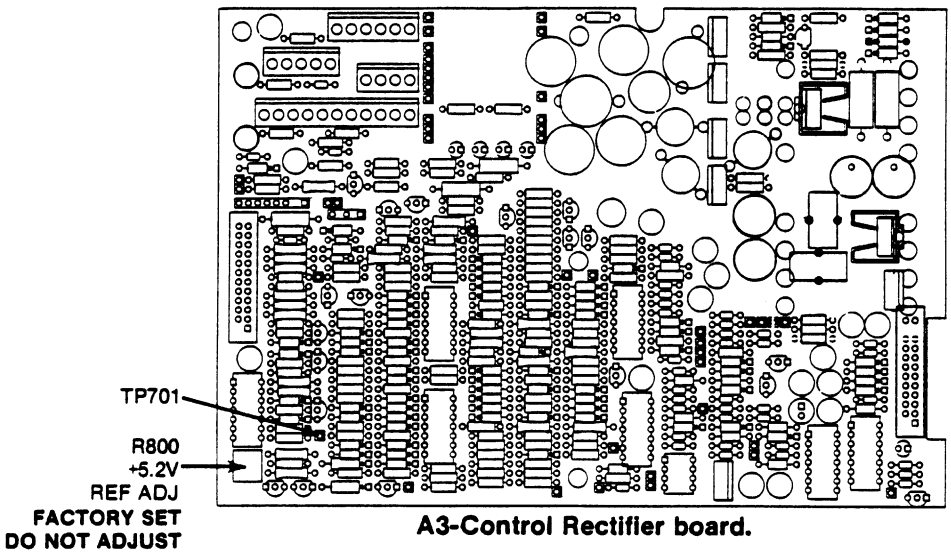
  MCALCONSTANTS 134:XXXX (where XXXX is the cal constant number loaded into NV RAM.

h. Remove the Term Conn Link (shorting strap) from the CAL-LOCK terminals on the A6 Time Base board.

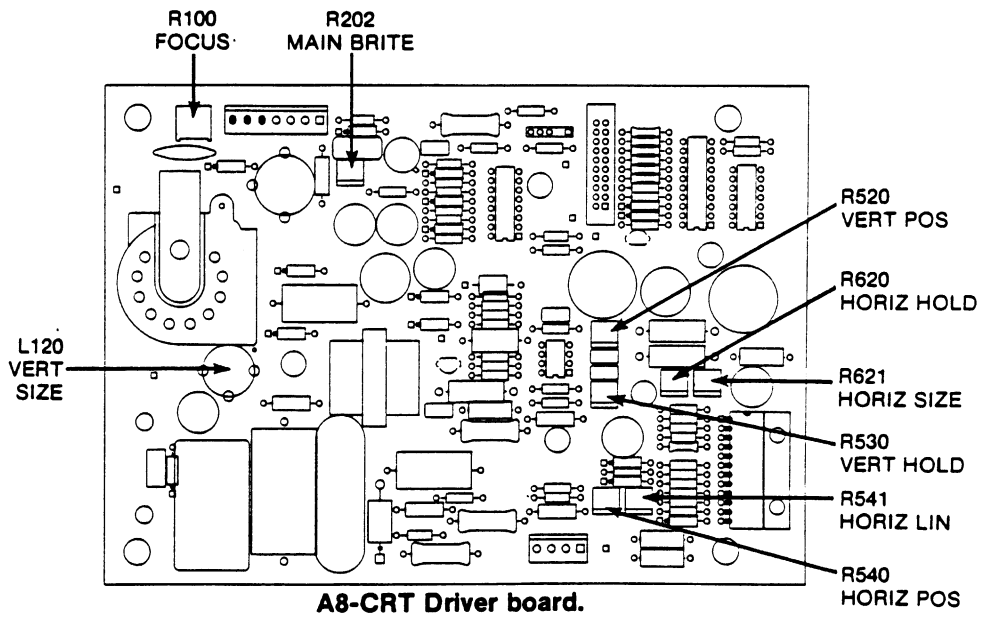
i. This completes the Adjustment Procedure.



A4-Regulator board.

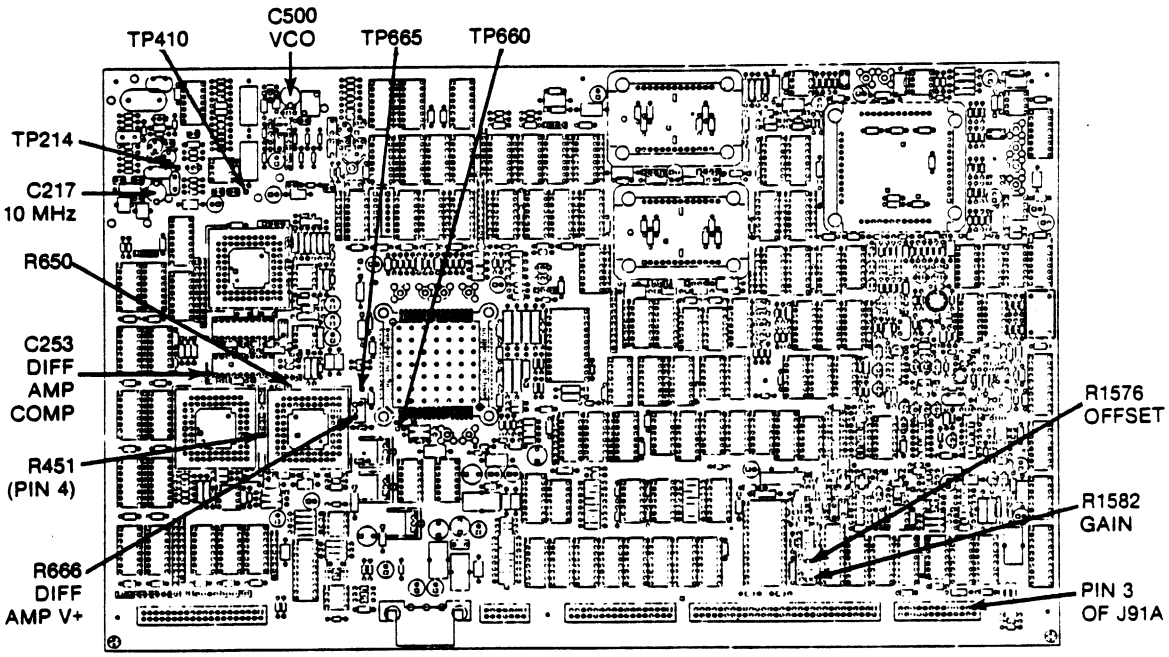


A3-Control Rectifier board.

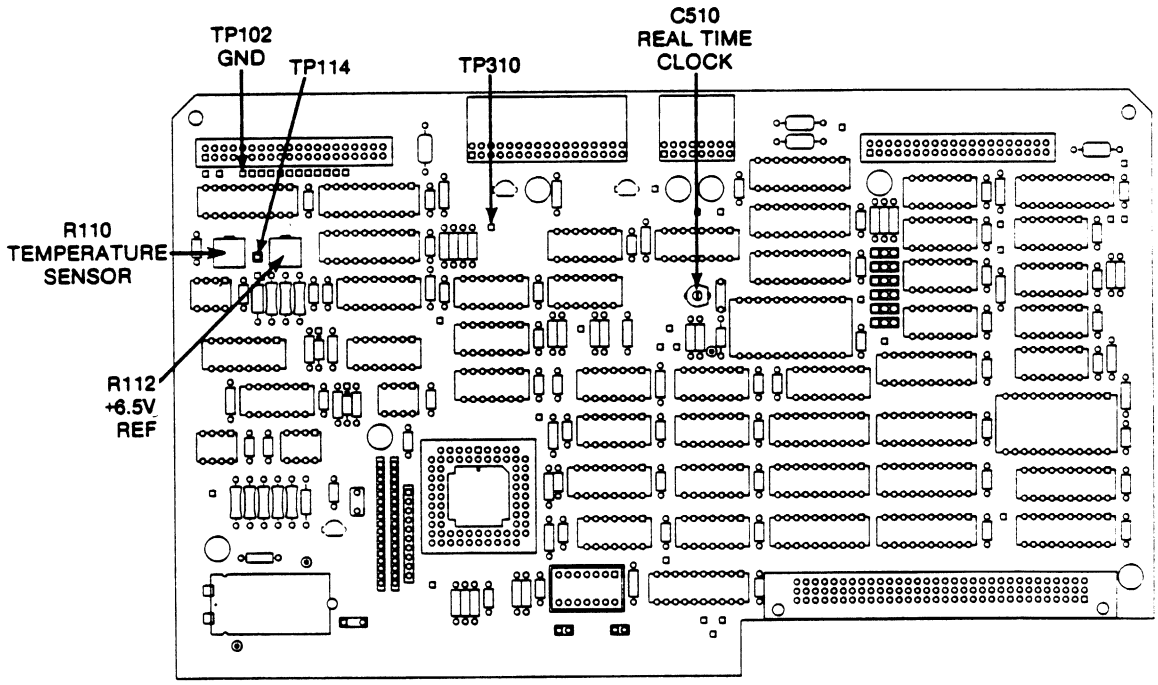


A8-CRT Driver board.

FIGURE A

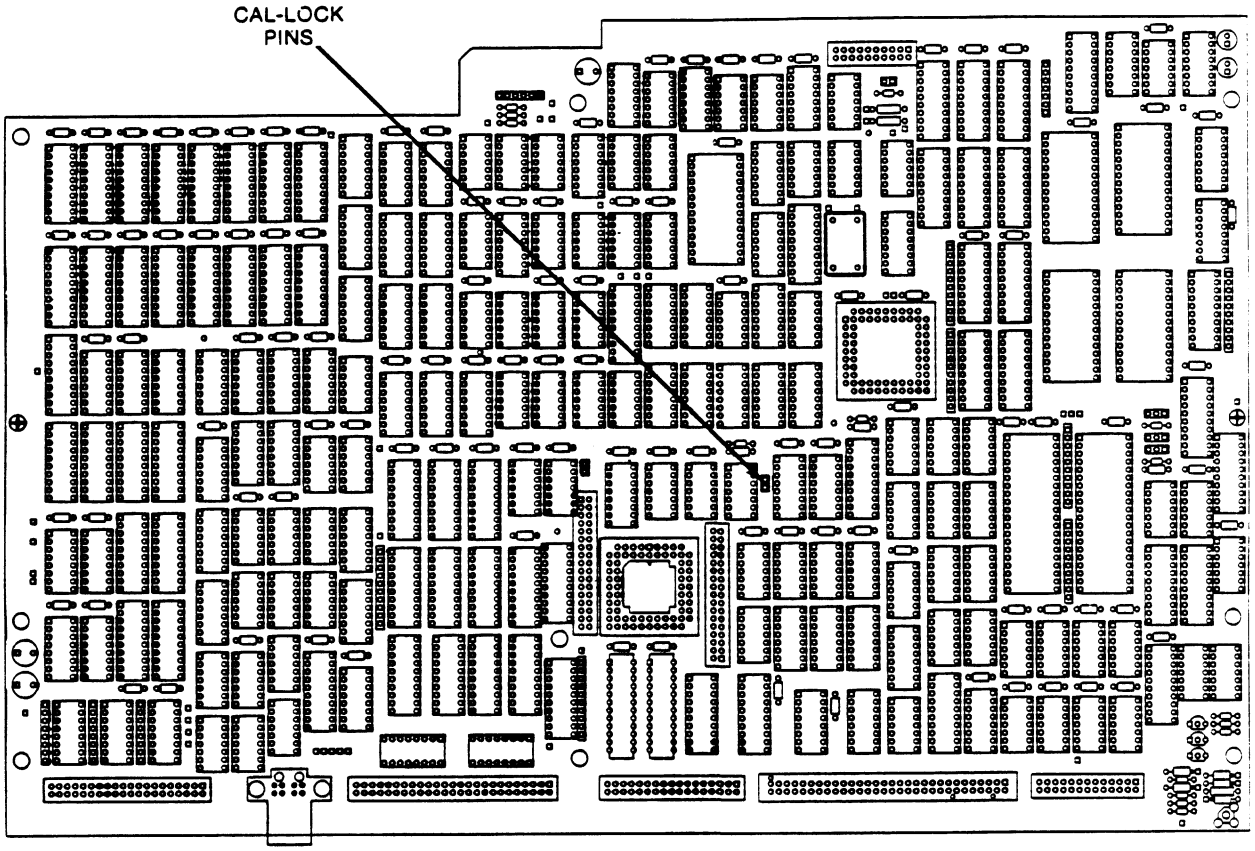


A5-Acquisition board.



A14-Input/Output board.

FIGURE B



A6-Time Base board.

FIGURE C

Part 4
Maintenance

Preliminary
Maintenance

This section of the manual contains information for performing preventive maintenance, and corrective maintenance for the 11401/11402 Oscilloscopes.

Preventive Maintenance

Preventive maintenance, performed regularly, can prevent instrument breakdown and may improve the reliability of the instrument. The severity of the environment to which the instrument is subjected will determine the frequency of maintenance. A convenient time to perform preventive maintenance is preceding electrical adjustment of the instrument.

Cabinet Panel Removal

WARNING

Dangerous potentials exist at several points throughout this instrument. When the instrument is operated with the covers removed, do not touch exposed connections or components. Some transistors have voltages present on their cases. Disconnect power before cleaning the instrument or replacing parts.

The top and bottom cabinet panels provide protection from operating potentials present within the instrument. In addition, they reduce radiation of electromagnetic interference from the instrument. Screws retain the cabinet panels. To remove the panels, remove the screws and lift the panels off. Operate the instrument with the panels in place to protect the interior from dust.

Cleaning

The 11401/11402 should be cleaned as often as operating conditions require. Accumulation of dirt in the instrument can cause overheating and component breakdown. Dirt on components acts as an insulating blanket and prevents efficient heat dissipation. It also provides an electrical conduction path which may result in instrument failure. The side panels reduce the amount of dust reaching the interior of the instrument. Operation without the panels in place necessitates more frequent cleaning.

CAUTION

Avoid the use of chemical cleaning agents which might damage the plastics used in this instrument. Exercise care when cleaning Hypcon connectors; see cleaning instructions under Hypcon Connectors in this section. Use a nonresidue type of cleaner, preferably isopropyl alcohol or totally denatured ethyl alcohol. Before using any other type of cleaner, consult your Tektronix Service Center or representative.

Exterior

Loose dust accumulated on the outside of the instrument can be removed with a soft cloth or small brush. The brush is also useful for dislodging dirt on and around the front-panel controls. Dirt which remains can be removed with a soft cloth dampened in a mild detergent and water solution. Do not use abrasive cleaners.

Crt

Clean the crt faceplate with a soft, lint-free cloth dampened with denatured alcohol.

Interior

Cleaning the interior of the instrument should only be occasionally necessary. The best way to clean the interior is to blow off the accumulated dust with dry, low-velocity air (approximately 5 lb/in2. Remove any dirt which remains with a soft brush or a cloth dampened with a mild detergent and water solution. A cotton-tipped applicator is useful for cleaning in narrow spaces, or for cleaning more delicate circuit components.

CAUTION

Circuit boards and components must be dry before applying power to prevent damage from electrical arcing.

The high-voltage circuits should receive special attention. Excessive dirt in this area may cause high-voltage arcing and result in improper instrument operation.

Visual Inspection

The 11401/11402 should be inspected occasionally for such defects as broken connections, improperly seated semiconductors, damaged or improperly installed circuit boards, or improperly installed circuit boards, and heat-damaged parts. The corrective procedure for most visible defects is obvious; however, particular care must be taken if heat-damaged parts are found. Overheating usually indicates other trouble in the instrument; therefore, correcting the cause of overheating is important to prevent recurrance of the damage.

Semiconductor Checks

Periodic checks of semiconductors are not recommended. The best check of semiconductor performance is actually operation in the instrument. More details on semiconductors are given later in this section.

Periodic Electrical Adjustment

To ensure accurate measurements, check the electrical adjustment of this instrument after each 1000 hours of operation, or every twelve months if used infrequently. In addition, replacement of components may necessitate adjustment of the affected circuits. Complete adjustment instructions are given in Section 3, Adjustment Procedure. This procedure can be helpful in localizing certain troubles in the instrument, and in some cases, may correct them.

TABLE 1
Adjustments Required after Circuit Board or Module Replacement

Circuit Board or Module Replaced	No Adjustment Required	Adjustments Required	Information
A1 Plug-In Interface	✓		
A2A1 Line Inverter		+5 V Ref (A3R800) Reg Ref (A4R830)	
A2A2 Control Rectifier		+5 V Ref (A3R800) Reg Ref (A4R830)	
A4 Regulator		Reg Ref (A4R830)	
A5 Acquisition		Offset (A5R1576) Gain (A5R1582)	
A6 Time Base*	✓		
A7 Display Controller*	✓		
A8 Crt Driver		Main Brite (A8R202) Horiz Hold (A8R620) Vert Hold (A8R530) Vert Pos (A8R520) Vert Size (A8L120) Horiz Lin (A8R541) Horiz Size (A8R621) Horiz Pos (A8R540) Focus (A8R100)	
A9 Touch Panel	✓		
A10 Front Panel Control	✓		
A12 Rear Panel	✓		
A13 Mother	✓		
A14 I/O		Time/Date	Refer to the 11401/11402 User's Reference Manual, page 2-206.
A15 MMU	✓		
A16 Compressor	✓		

*These circuit boards contain firmware. If the board is replaced, refer to the firmware update instructions that accompany the replacement board.

TABLE 1 (cont)
Adjustments Required after Circuit Board or Module Replacement

Circuit Board or Module Replaced	No Adjustment Required	Adjustments Required	Information
A17 Main Processor*		STEP 1.	If the firmware version of the new board is different from that of the old board, you must update the A18 Memory Processor board's firmware to the same version.
		STEP 2. Clear NV RAM	Remove the Battery Backup Disable jumper J150, located on the A17 Main Processor board. Connect a shorting wire across capacitor C150 (also located on the A17 Main Processor board) for approximately 15 seconds. Remove shorting wire and replace the Battery Backup Disable jumper on J150.
		STEP 3. Install Unit ID	Refer to the 11401/11402 User's Reference Manual, page 3-137.
		STEP 4. Install Cal Constant	Refer to Step D, Sampler and Digitizer in the Adjustment Procedure.
A18 Memory*	✓		If the firmware version of the new board is different from that of the old board, you must update the A17 Main Processor board's firmware to the same version.
CRT		Main Brite (A8R202) Horiz Hold (A8R620) Vert Hold (A8R530) Vert Pos (A8R520) Vert Size (A8L120) Horiz Lin (A8R541) Horiz Size (A8R621) Horiz Pos (A8R540) Focus (A8R100)	
Power Module		+5 V Ref (A3R800) Reg Ref (A4R830)	

*These circuit boards contain firmware. If the board is replaced, refer to the firmware update instructions that accompany the replacement board.

Corrective Maintenance

Corrective maintenance consists of component replacement and instrument repair. Special techniques required to replace components in the 1140Ø1/1140Ø2 Oscilloscope mainframes are given here.

Contents

The following instructions and disassembly procedures will be covered in this section:

Power Supply Voltage Hazard

If you must work inside the power supply with power applied, be careful to **not** touch any metal part on the A2 Line Inverter Board. The metal frame of the power supply chassis itself should be safe to touch. (However, a live circuit **could** short to the chassis, under certain conditions, and then the chassis would be dangerous to handle).

WARNING

All metal components, including any metal-faced ones, on the A2 Line Inverter Board should be considered hazardous. *This is because these components are at the AC line voltage potential.*

Always remove the line power cord before any disassembly is begun.

An electric-shock hazard exists when the 11401/11402 is NOT grounded. Do not remove the ground wire (green-yellow) that connects the power supply chassis to the mainframe.

Manually discharge the line storage capacitors on the A2 Line Inverter Board before beginning any work inside the power supply. *(See the* ***Access to Components in the Power Supply*** *procedure, in this section).*

Obtaining Replacement Parts

All electrical and mechanical part replacements for the 11401/11402 can be obtained through your Tektronix Field Office or representative. However, many of the standard electronic components can be obtained locally in less time than is required to order them from Tektronix, Inc. Before purchasing or ordering replacement parts, check the parts list for value, tolerance, rating and description.

NOTE

When selecting replacement parts, remember that the size and shape of a component may affect its performance in the instrument. All replacement parts should be direct replacements unless you know that a different component will ***not*** *adversely affect instrument performance.*

Special Parts

Some parts are manufactured or selected by Tektronix, Inc. to satisfy particular requirements. Some are manufactured for Tektronix, Inc. to satisfy our specifications. Most of the mechanical parts used in this instrument have been manufactured by Tektronix, Inc. To determine manufacturer of parts, refer to Parts List, Cross Index Mfr. Code Number to Manufacturer.

Ordering Parts

When ordering replacement parts from Tektronix, Inc., include the following information:

1. Instrument type.
2. Instrument serial number.
3. A description of the part (if electrical, include circuit number).
4. Tektronix Part Number.

Soldering Techniques

WARNING

To avoid electric-shock hazard and instrument damage, disconnect the instrument from its power source before soldering.

The reliability and accuracy of the 11401/11402 can be maintained only if proper soldering techniques are used when repairing or replacing parts.

The desoldering and removal of parts is especially critical and should be done only with an anti-static vacuum solder extractor; preferably, one approved by a Tektronix, Inc. Service Center.

Use wire solder with rosin core, 63% tin, 37% lead. Contact your local Tektronix, Inc. representative or field office for approved solders.

All circuit boards used in the 11401/11402 are multilayer. Conductive paths between the top and bottom layers may connect with one or any number of inner layers. If this inner conductive path is broken (due mainly to poor soldering practices), the board is unusable and must be replaced. **Damage can void warranty.**

CAUTION

Only an experienced maintenance person, proficient in the use of vacuum-type desoldering equipment, should attempt repair of any board in this instrument.

When soldering on circuit boards or small wiring, use only a 15-watt, pencil-type soldering iron. A higher wattage soldering iron can cause the etched circuit wiring to separate from the board base material. It can also melt the insulation from small wiring. Always keep the soldering-iron tip properly tinned to ensure the best heat transfer to the solder joint. Apply only enough heat to make a good solder joint. To protect heat-sensitive components, hold the component lead with a pair of long-nose pliers between the component body and the solder joint.

The following technique should be used to replace components on the circuit boards.

Touch the tip of the vacuum desoldering tool directly to the solder to be removed.

CAUTION

Excessive heat can cause the etched circuit wiring to separate from the board base material.

Never allow the solder extractor to remain on the board for more than three (3) seconds. Solder wick, spring-actuated or squeeze-bulb solder suckers, and heat blocks (for multi-pin components) must **not** be used. **Damage can void warranty.**

NOTE

Machine insertion of some components places a bend in both of the leads. These bent leads hold the component in position during a flow-solder manufacturing process which solders all of the components at once. ***Some components are difficult to remove due to their bent leads.*** *To make removal of machine-inserted components easier, first remove the solder from the joint. Then straighten the leads of the components on the back of the circuit board, using a small screwdriver or pliers. Next, remove the component.*

When removing multi-pin components, do not heat adjacent conductors consecutively (see Fig. 6100-301). **Pause a moment to allow the circuit board to cool before proceeding to the next pin.**

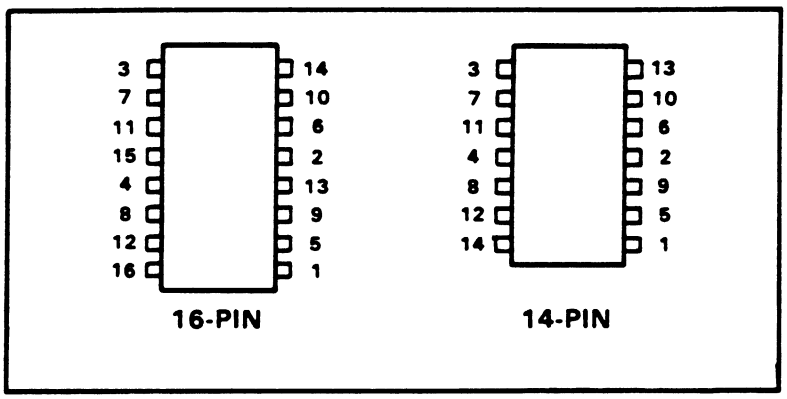


Figure 6100-301. Recommended IC desoldering sequence.

Bend the leads of the replacement components to fit the holes in the circuit board. Insert the leads into the holes in the board, or as originally positioned.

Touch the iron to the connection and apply enough solder to make a firm solder joint.

Cut off any excess lead protruding through the board.

Clean the areas around the solder connection with a flux-removing solvent. Be careful not to remove the information printed on the circuit board.

CAUTION

Before cleaning around HYPCON connectors, read the instructions about them. See the Semiconductors procedure, in this section.

TABLE 3-1
REFERENCE FOR SUPPORT ITEMS

Purpose	Item	Qty. Req.	Location
Circuit Board Removal Tools	Phillips Screwdriver, No. 1	1	Removing and Replacing, Circuit Boards
	Phillips Screwdriver, No. 2	1	
	Torx screwdriver, No. 7	1	
	Torx screwdriver, No. 8	1	
	Torx screwdriver, No. 10	1	
	Torx screwdriver, No. 15	1	
	Allen wrench, 1/16"	1	
	Nutdriver, 3/16"	1	
	Nutdriver, 1/4"	1	
	Nutdriver, 7/16"	1	
	Pliers, needle-nose	1	
	Soldering iron, 15W	1	
	Vacuum Solder extractor, anti-static	1	
	Torque wrench, 0-10" pound range	1	
	Resistor, shorting (See Fig.6100-308)	1	
Optional Tools	Flashlight, penlight size	1	Removing and Replacing, Circuit Boards

Removing and Replacing Parts

WARNING

*To avoid electric-shock hazard and instrument damage, **always disconnect the instrument from its power source before removing or replacing components or plug-in units.***

The exploded-view drawings associated with the Replaceable Mechanical Parts List may be helpful in the removal or disassembly of individual components or subassemblies.

Addendum:

The top and/or bottom covers will need to be removed for most repairs. Such removal is not mentioned in each procedure. As the covers would need to be removed before the individual circuit boards are located, it is to be assumed that they were off the instrument.

Whenever a specific area is mentioned (such as the right side), it will usually be in reference to the front of the 11401. If another reference is intended, it will be so described (such as the left side, as facing the rear).

NOTE

Refer to the "Adjustment After Repair" procedure, at the end of this section.

Power Supply Removal

The power supply can be slid out of the rear of the 1140l/1140Ø2 for maintenance and troubleshooting. It may also be removed to gain better access to the A1 Plug-In Interface Board, the A2 Line Inverter Board, the A3 Control Rectifier Board or the A4 Regulator Board.

To remove the power supply from the mainframe, proceed as follows:

- Turn the mainframe on its left side (as viewed facing the rear panel). The power supply will now be at the bottom of the instrument.
- Remove the eight Torx-head screws that secure the power supply (see Fig. 6100-302).

(REFER TO TABLE 1 AT THE END OF THIS SECTION.)

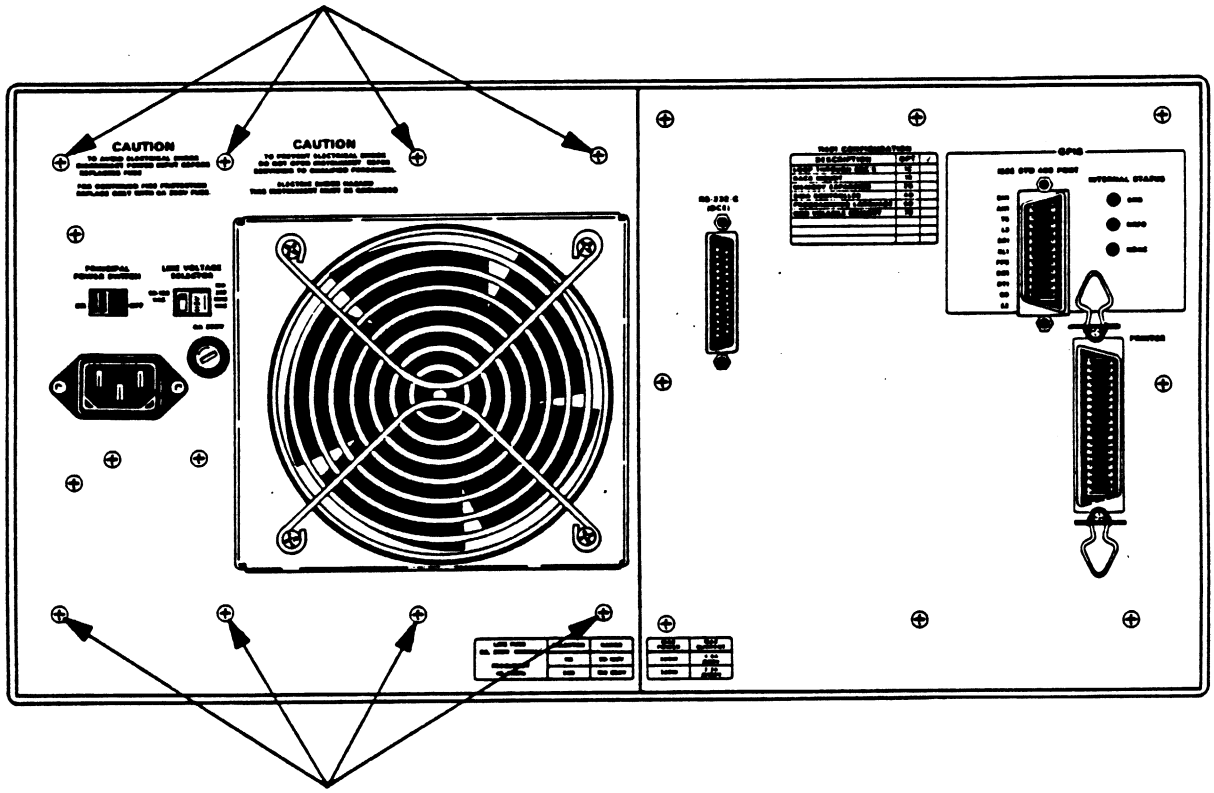


Figure 6100-302. Rear panel location of screws securing the power supply.

- Carefully pull the power supply part way out of the mainframe. Stop before the wires (to the A3 Control Rectifier Board connectors) begin to stretch taut or bind.

CAUTION

Excessive pulling on the power supply beyond this point may damage connector pins.

- The wires should be long enough to permit the power supply to be partially removed from the mainframe without disconnecting any wire connectors.

NOTE

Should disconnection of any wires be necessary, record their location for correct replacement. (See Fig. 6100-304).

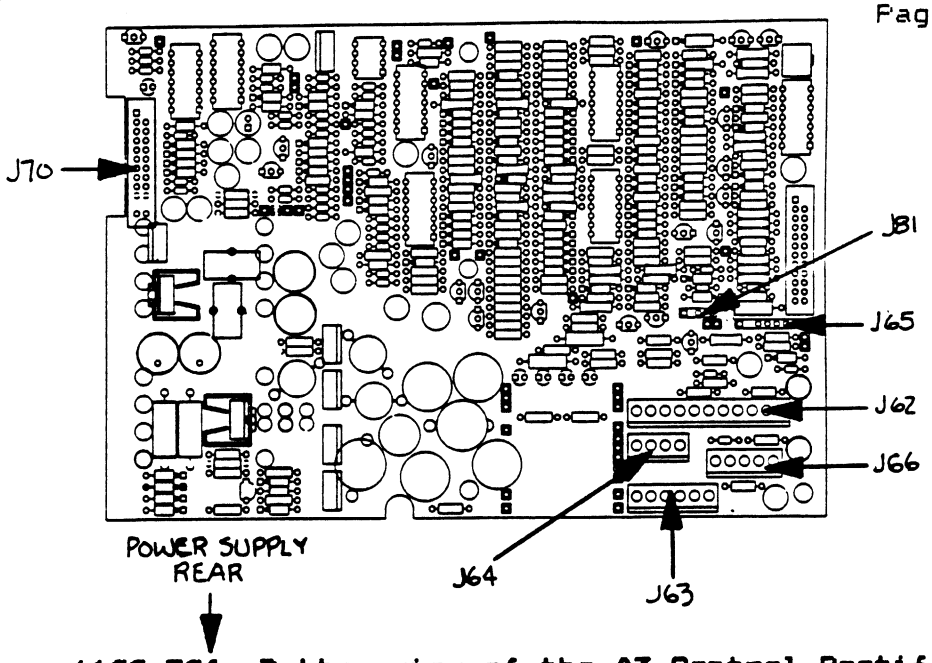


Figure 6100-304. Bottom view of the A3 Control Rectifier Board showing connector locations.

- Do not remove the chassis ground (green-yellow) wire. It should stay attached between the power supply and the mainframe.

  The power supply may now be removed from the mainframe. First remove the wire connectors from their pins on the A3 Control Rectifier Board. Depending on the repair work to be done, it may be appropriate to set both the detached power supply and the mainframe right-side up.

- To apply power, attach the A.C. power cord to the power plug receptacle.

NOTE

The fan will revolve slightly slower than normal when the instrument is connected this way.

This connection will allow troubleshooting the power supply and/or power-related problems in the mainframe.

NOTE

Before removing any of the power supply covers, read the warnings in the ***Access to Components in the Power Supply procedure*** *of this section.*

To replace the power supply, follow the previous procedure in reverse order.

NOTE

Align the metal guides on the top of the power supply with the grooves inside the upper part of the opening in the mainframe.

Be careful not to pinch any wires or interconnecting cables while installing the power supply.

Replace the eight Torx-head screws into the rear plate and tighten them securely.

Access to Components in the Power Supply

To reach the components inside the power supply chassis for maintenance or repair, use the following procedure:

WARNING

Disconnect the 11401/11402 from the power source. ***Allow the line storage capacitors to discharge before removing any cover from the power supply.*** *Unless they are manually discharged, these capacitors remain charged with a high dc voltage for several minutes after the line power is disconnected.* ***A warning-indicator (neon bulb) located on the A2 Line Inverter Board flashes when this stored voltage exceeds about 80 volts. Do not remove the power supply covers while this light is flashing.***

1. Remove the power supply as previously described.

   a. Disconnect the A.C. power cord before proceeding.

2. To reach the A2 Line Inverter Board, first remove the protective cover from the top of the power supply chassis. This is done by removing the four screws securing the cover.

   a. Carefully slide the protective cover off the power supply chassis.

   b. The A2 Line Inverter Board is now accessible for maintenance or repair. However, if the 11401/11402 is to be operated with the cover removed, heed this:

WARNING

All metal components on the A2 Line Inverter Board should be considered hazardous. *Such components remain at the AC line voltage potential.*

Once the power cord has been disconnected, manually discharge the line storage capacitors. (See Fig. 6100-307).

c. Before starting maintenance or taking resistance measurements, manually discharge the line storage capacitors (C200, C220, C310 and C320) as follows:

- Remove the protective cover as previously described.
- Locate the line storage capacitors on the A2 Line Inverter Board. Place a 100-200 ohm, 400 volt, 1-watt insulated resistor in parallel with R220 (470 KΩ) to discharge the capacitors, see Fig. 6100-307. For an example of this shorting resistor, see Fig. 6100-308.

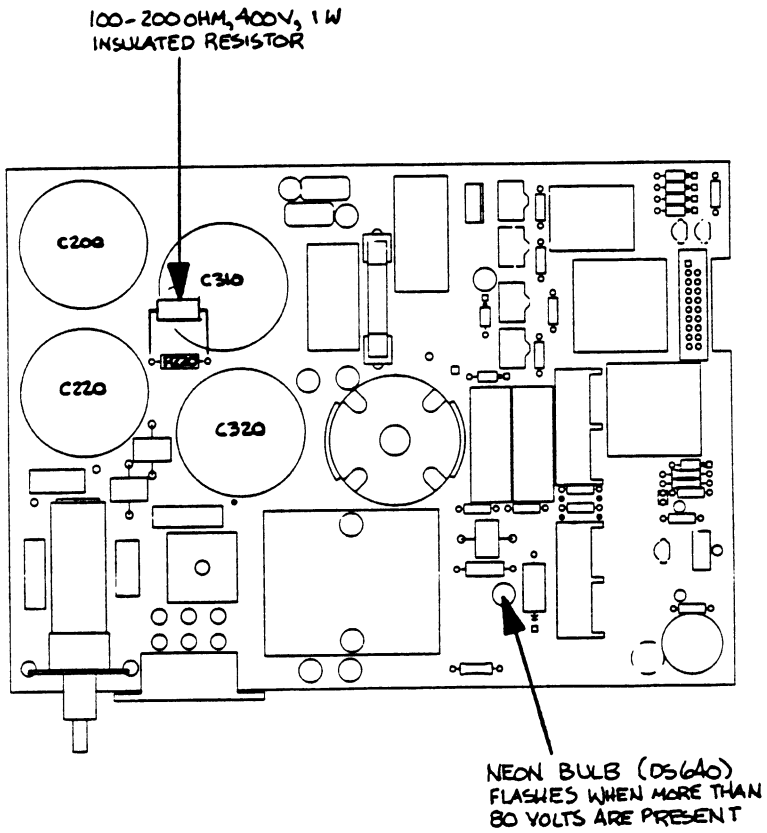


Figure 6100-307. Manually discharging the line storage capacitors on the A2 Line Inverter Board.

NOT AVAILABLE AT THIS TIME

Figure 6100-308. Resistor used to discharge line storage capacitors across A2R220.

3. To replace the power supply protective cover, follow the removal procedure in reverse order.

4. To reach the line voltage circuitry (Principal Power Switch, Line Voltage Selector, fuseholder, etc.), proceed as follows:

   a. Remove the two long screws from the right side of the fan housing (as viewed facing the rear panel). (See Fig. 6100-302).

   b. Remove the screw above and left of the Principal Power switch. Then remove the screw below and left of the power plug receptacle (the one closest to the left edge).

   c. Follow step 3 of the A2 Line Inverter Board Removal procedure, later in this section.

      - Remove the overall cover from the power supply.

   d. To replace the overall cover, reverse this procedure.

5. Complete access to the A3 Control Rectifier Board or to the A2 Line Inverter Board may be obtained by following the procedures to remove these boards. (See ''Circuit Board Removal'' in this section).

6. Replace the power supply as previously described.

NOTE

Check that no wires contact the fan blades.

Fan Motor Removal

Remove and replace the fan motor as follows:

1. Mark the top of the fan motor housing. (It reassembles only one way). Remove the four screws holding the assembly together. (See Figure 6100-302).

   - Hold the housing as the last screws are removed.

2. Separate the grill and the housing from the motor.

3. Remove the two wires at their motor connections.

   - Note that the red wire is (+) and the brown wire is (-).

4. Remove the fan motor.

NOTE

Observe the position in which the motor was mounted. Replace it the same way, or the fan wires may not reach.

5. To replace the fan motor, reverse the order of removal.

   - Don't pinch the wires under the fan housing.

   - Tighten screws securely. Remove the marking from the top of the housing.

   - Check that no wires contact the fan blades.

Cathode-Ray Tube Removal

Remove the cathode-ray tube (crt) as follows:
(REFER TO TABLE 1 AT THE END OF THIS SECTION)

WARNING

The crt may retain a dangerous electrical (12 kV) charge. Before removing the crt, the anode must be fully discharged. ***Short the anode lead from the crt to the chassis. Wait approximately ten minutes and again firmly short this lead to the chassis.*** *Then, remove the crt.*

Use care when handling. Breakage of the crt causes a high-velocity scattering of glass fragments (implosion). Protective clothing and safety glasses should be worn. Avoid striking the crt on any object which might cause it to crack or implode. When storing a crt, place it in a protective carton. Otherwise, set it face down in a protected location. Be certain it is on a smooth surface with a soft mat under the crt faceplate.

1. Turn the 11401/11402 so that its front is at your right. Remove the two flat, torx-head screws holding the crt shield to the chassis.

2. Lift up the outside of the shield.

   - The inner edge of the shield is held in place by two tabs. These fit into slots in the chassis beneath the inner edge of the A7 Display Controller board.

   As the shield is lifted, its bottom will clear the frame behind the instrument's handle. At that point, remove the shield carefully. Don't allow it to strike the crt.

3. Use a non-conducting tool to pry up the rubber cap of the anode lead. (It is on the upper part of the crt behind the front casting. See Fig. 6100-311. Release the spring clip inside the cap and in the crt opening to remove the anode.

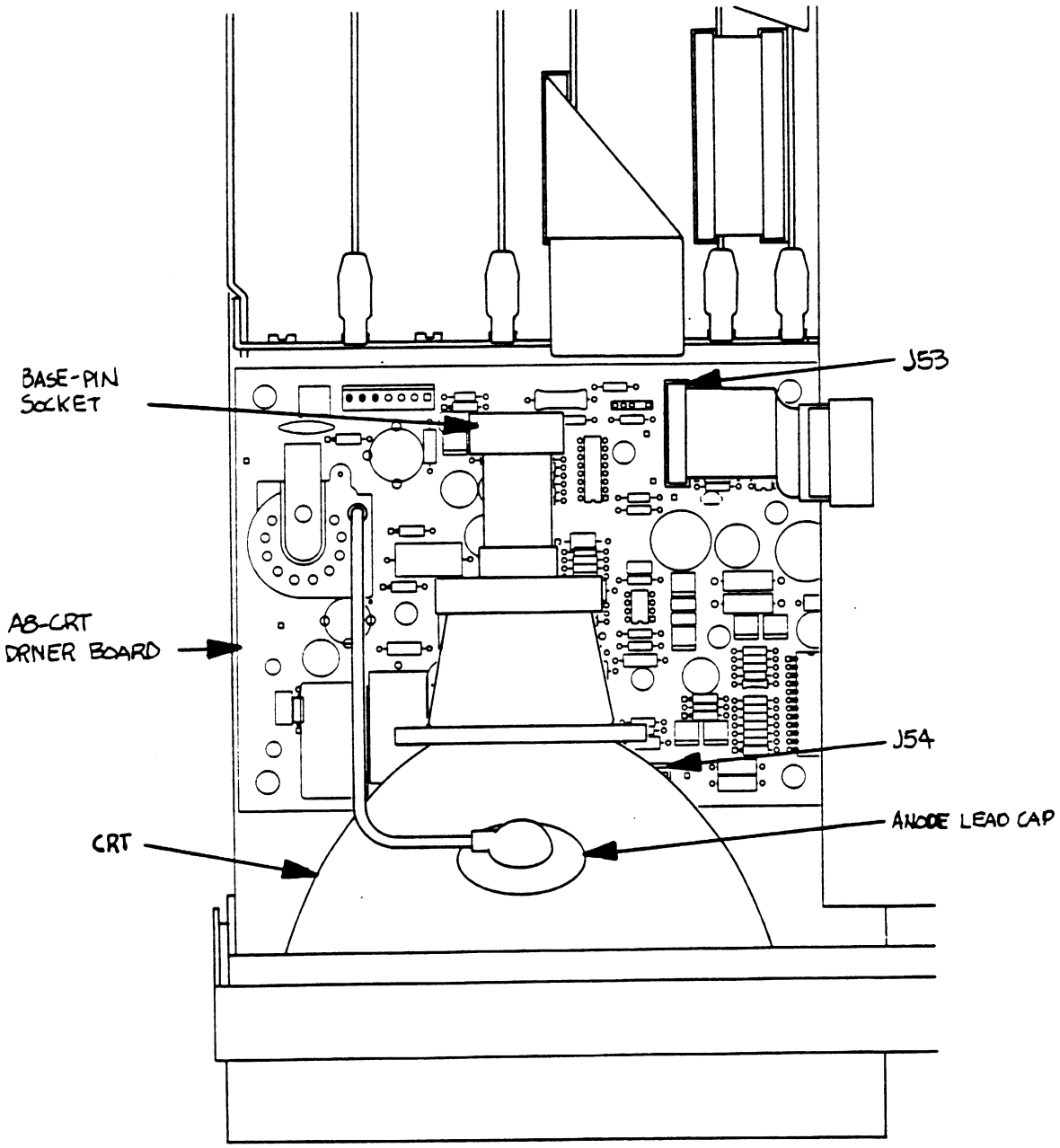


Figure 6100-311. Top view of CRT and A8-CRT Driver Board.

WARNING

CRT anode voltage is 12 kV. Ground the lead to the chassis to short any stored charge remaining in the crt.

Wait about ten minutes and ground the anode lead again.

4. Remove the base-pin socket from the rear of the crt. Install a protective cap over the pins.

5. Disconnect connector J54 from the A8 CRT Driver Board. It is located on the right front side, as viewed facing the crt. (See Fig. 6100-311).

6. Turn the mainframe on its right side. The crt will be at the top.

7. Remove the two flat-head screws from the bottom of the bezel. Turn the mainframe right side up.

8. Remove the two Control knobs from the front of the bezel. (Use an allen wrench to loosen the knob setscrews).

9. Lift up on the bottom of the bezel and swing it outward.

NOTE

The upper part of the bezel is held by two tabs. These tabs fit into two slots inside the front casting.

10. Remove the bezel.

CAUTION

Be careful not to damage the interconnecting cable to P73.

To protect it from being scratched, or marred, cover the front of the bezel with some protective material.

11. Remove the four Torx-head screws and washers from the corner prongs of the band fastened to the faceplate.

CAUTION

Don't allow the crt to drop when loosening screws.

12. Hold one hand on the faceplate. Gently push forward on the crt base with the other hand. Slowly remove the crt from the front of the 11401/11402.

Cathode-Ray Tube Replacement

Replace the crt as follows:

1. Replace connector J54 on the A8 Crt Driver Board (see Fig. 6100-311).

2. Insert the crt into the front casting with the anode opening towards the top. Align the corner prongs of the faceplate band evenly around the four screwholes near the faceplate corners. Replace the four Torx-head screws and washers. Tighten securely.

3. Clean the crt faceplate with a glass cleaner and a soft lint-free cloth. Be careful not to scratch the glass.

4. Replace the front-panel bezel. Insert the two tabs at the top of the bezel into the slots inside the front casting, above the upper edge of the faceplate. At the same time, center the two holes (near the bottom right) of the bezel around the shafts for each control knob. Push the bottom of the bezel backwards until it fits flush against the casting and in the side grooves of the casting. Don't pinch the interconnecting wire cable.

5. Replace the two control knobs on their shafts. Tighten their setscrews securely.

6. Turn the mainframe on its right side. (The crt will be at the top). Replace the two flathead screws in the bezel and tighten securely.

7. Turn the mainframe right side up.

8. Remove the protective cap from the crt base pins. Install the crt base-pin socket. Align the keyway of the socket with the gap between the pins on the base. Push the socket over the crt pins until it is seated.

9. Install the anode lead in the hole near the top of the crt. Inside the rubber cap is a spring clip. Put one side of the clip into the crt hole, then push the other side in. Check that the clip is connected by lightly tugging on the cap.

10. Replace the crt shield. Insert the two tabs on the shield's inner edge into their respective slots in the chassis. These slots are underneath the A7 Display Controller Board.

    - Slide the outer edge of the shield behind the handle and inside the chassis. Align the countersunk holes with the pem-nuts on the inside of the shield.

11. Reinstall the two flathead, Torx-head screws. Tighten them securely.

NOTE

Replacing the crt will require that the instrument be readjusted. Refer to the Checks and Adjustments procedures.

Lithium Battery Handling and Disposal

A Lithium battery is soldered on the A14 Input/Output Board (BT13Ø) and on the A17 Main Processor Board (BT16Ø).

NOTE

Record the polarity before removing the battery.

Remove the battery from the board by using the standard desoldering process. (See the **Soldering Techniques** procedures in this section). These batteries require special handling for disposal.

WARNING

To avoid personal injury, observe proper procedures for handling and disposal of Lithium batteries. ***Improper handling may cause fire, explosion, or severe burns. Don't recharge, crush, disassemble, heat the battery above 212 F (100 C), incinerate, or expose contents of the battery to water. Dispose of battery in accordance with local, state, and federal regulations.***

Typically, small quantities (less than 20) can be safely disposed of with ordinary garbage in a sanitary landfill.

Larger quantities must be sent by surface transport to a Hazardous Waste Disposal Facility. The batteries should be individually packaged to prevent shorting. Then, pack them into a sturdy container that is clearly labeled, ''Lithium Batteries--DO NOT OPEN''.

Replace the Lithium battery by reversing the order of removal. Observe that the polarity is correct.

Circuit Board Removal

All circuit boards used in the 11401/11402 Oscilloscope are multilayer. Conductive paths between the top and bottom layers may connect with one or any number of inner layers. If this inner layer conductive path is broken (due mainly to poor soldering practices), the board is unusable and must be replaced. **Damage can void warranty.**

If a circuit board is damaged beyond repair, replace the entire board assembly. Part numbers are given in the Replaceable Electrical Parts.

To determine the location of a circuit board, see the exploded view in Fig. 6100-313.

Most circuit boards in the 11401/11402 are mounted on the chassis. Pin connectors are used for electrical interconnection with chassis-mounted components and other circuit boards. Five boards (A14 I/O, A15 MMU, A16 Compressor, A17 Main Processor, and A18 Memory) plug onto the top of the A13 Mother Board. Feed-through connectors join the plug-on boards to the A13 Mother Board.

CAUTION

After removing a circuit board from the instrument, place it upon a non-conducting surface. *This will minimize the chance of static charge damage to the integrated circuits and/or related circuitry.*

Some parts mounted on a board must be retained for use with the new assembly. These parts would include interconnecting plugs, supports posts, and some wiring.

NOTE

Refer to the ***Adjustment After Repair procedure****, in this section.*

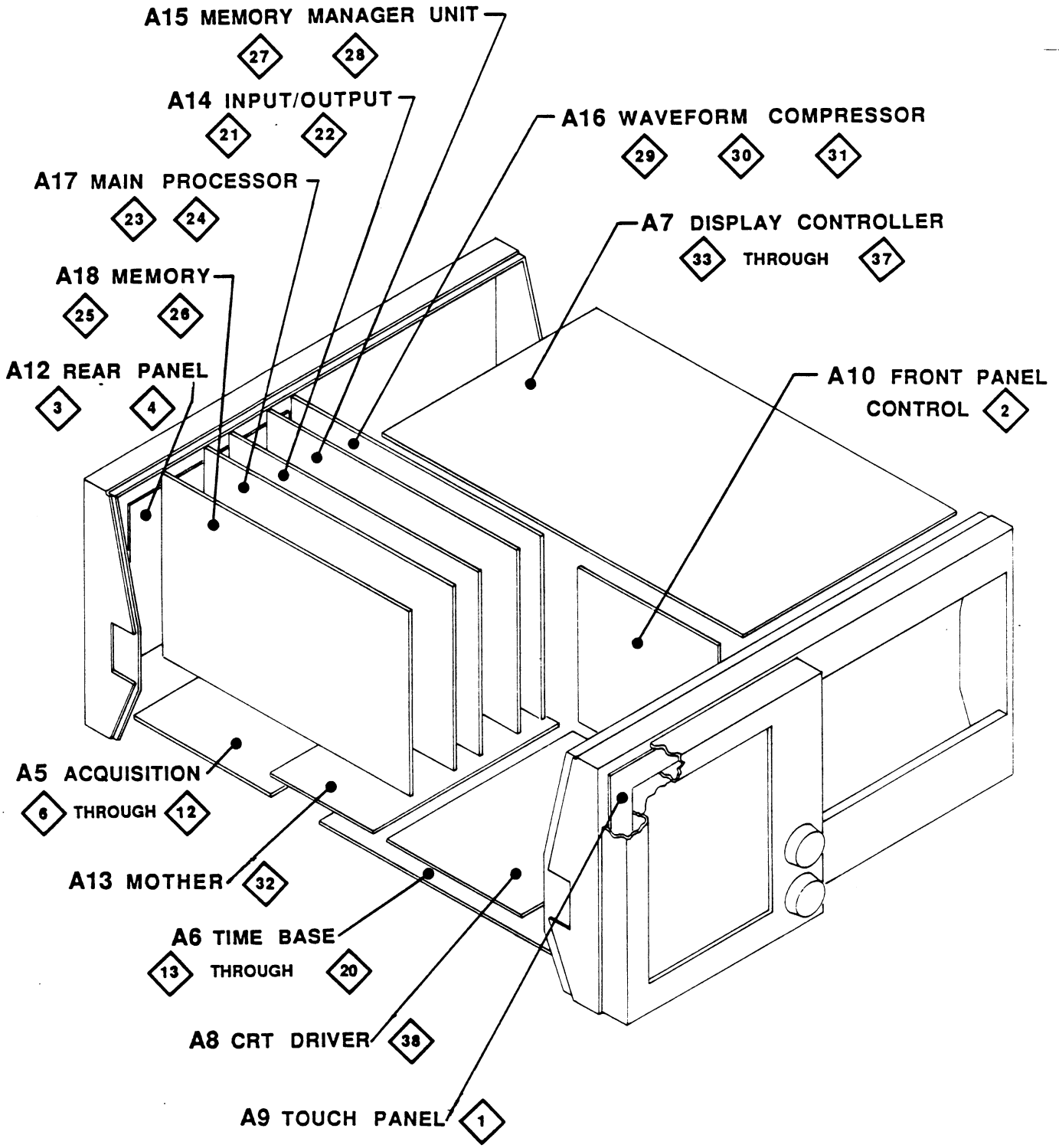


Figure 6100-313. Location of circuit boards in the 11401/11402.

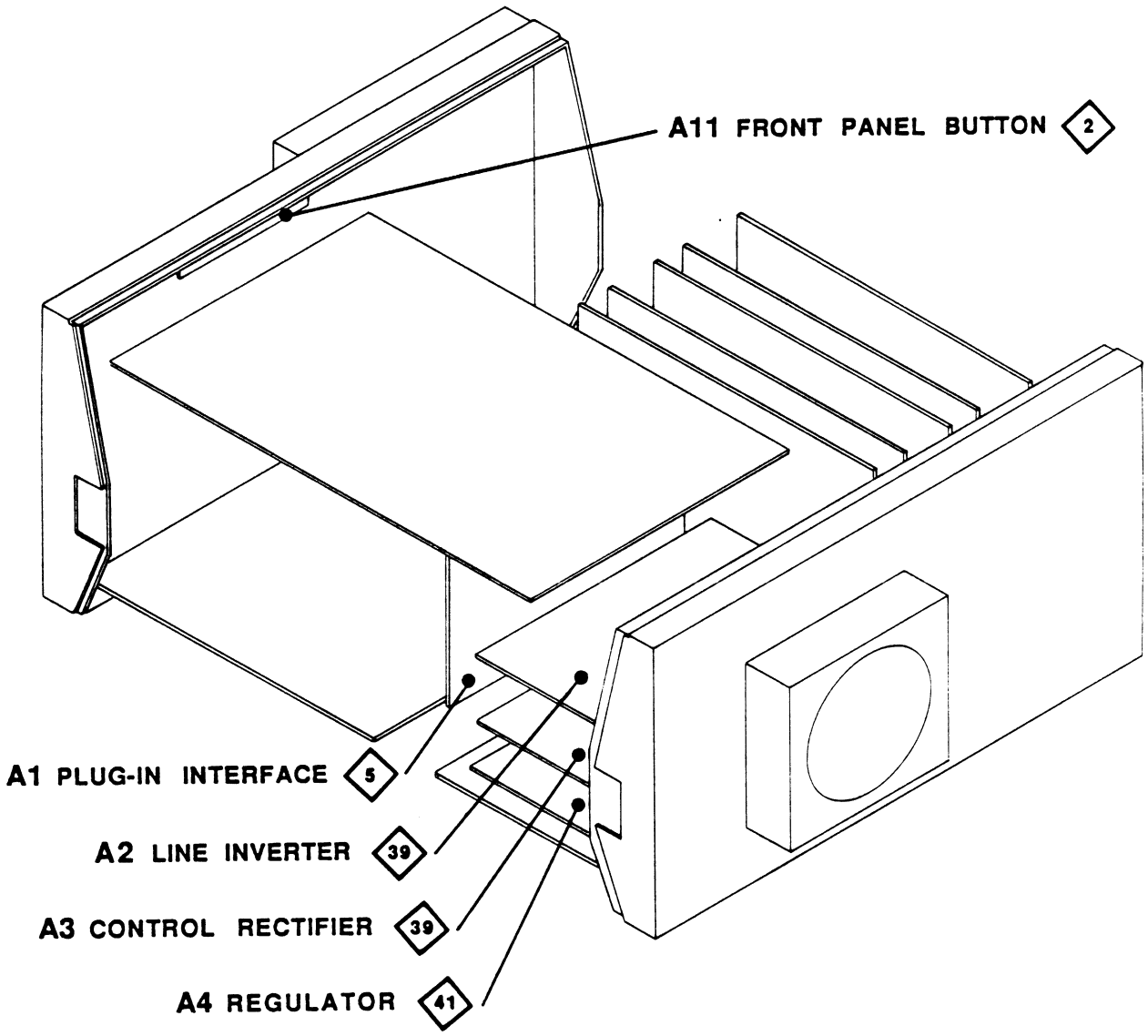


Figure 6100-313. (cont). Location of circuit boards in the 11401/11402.

Chassis-Mounted Boards

A1 Plug-In Interface Board

Remove and replace the A1 Plug-in Interface Board as follows:

1. Remove the plug-in units.

2. Remove the nine screws that fasten the three interface connector receptacles to the chassis. (See Fig. 6100-314).

3. Remove all the connectors from the A7 Display Controller board. Note the position of their index triangles so that the connectors can be correctly replaced. Remove the six Torx-head screws that fasten the board to the chassis. Remove the Display Controller Board. (See Fig. 6100-324 and "A7 Display Controller Board" later in this section).

4. Remove the Power Supply (see ''Power Supply Removal'', in this section). Remove the connectors from the A3 Control Rectifier Board, except for J81 (see "A3 Control Rectifier Board" in this section).

NOTE

Record the positions of the connectors for correct replacement.

Return the 11401/11402 to its right side up position (if the instrument is on its side).

5. Disconnect connectors J57 and J60 connectors from the A4 Regulator board (see Fig. 6100-315). Remove the two Torx-head screws from the metal heatsink at the rear of the board.

NOT AVAILABLE AT THIS TIME

Figure 6100-314. Plug-in compartment showing mounting screws for the A1 Interface Board.

NOT AVAILABLE AT THIS TIME

Figure 6100-315. Connector locations for removal of the A1 Interface Board.

NOTE

The A4 Regulator Board is now unfastened from the chassis. However, it still remains connected to the Plug-In Interface Board.

Carefully disconnect the J95 and J96 interconnecting pins from the Interface Board by pulling the Regulator board towards the rear. Remove the A4 Regulator Board.

6. Position the instrument so that the A1 Plug-In Interface Board can be removed through the top of the mainframe chassis.

7. Remove the A1 Plug-In Interface Board. Note the locations of the coaxial end-lead connectors and the interconnecting plugs so that they can be correctly replaced.

8. To replace the A1 Plug-In Interface Board, reverse the order of removal. Match the index triangle on the pin connectors to the corresponding triangle on the circuit boards or connectors. Correct location of the pin connectors is shown in the circuit board illustrations.

NOTE

To ease replacement of the screws in the Plug-In Interface connector receptacles (see Fig. 6100-314), start the screws when the Interface board is replaced into the instrument. Then, tighten all nine screws in the connector receptacles.

A2 Line Inverter Board

Remove and replace the A2 Line Inverter Board as follows:

1. Remove the power supply (see ''Power Supply Removal'', in this section).

2. Remove the protective cover from the power supply (see ''Access to Components in the Power Supply'', in this section. Follow steps 1 through 2a).

3. Remove the two screws that secure the Line Inverter Board (see Fig. 6100-317). Then remove the screw holding the front of the overall cover to the Line Inverter Board. Remove the two screws from the bottom front of that cover.

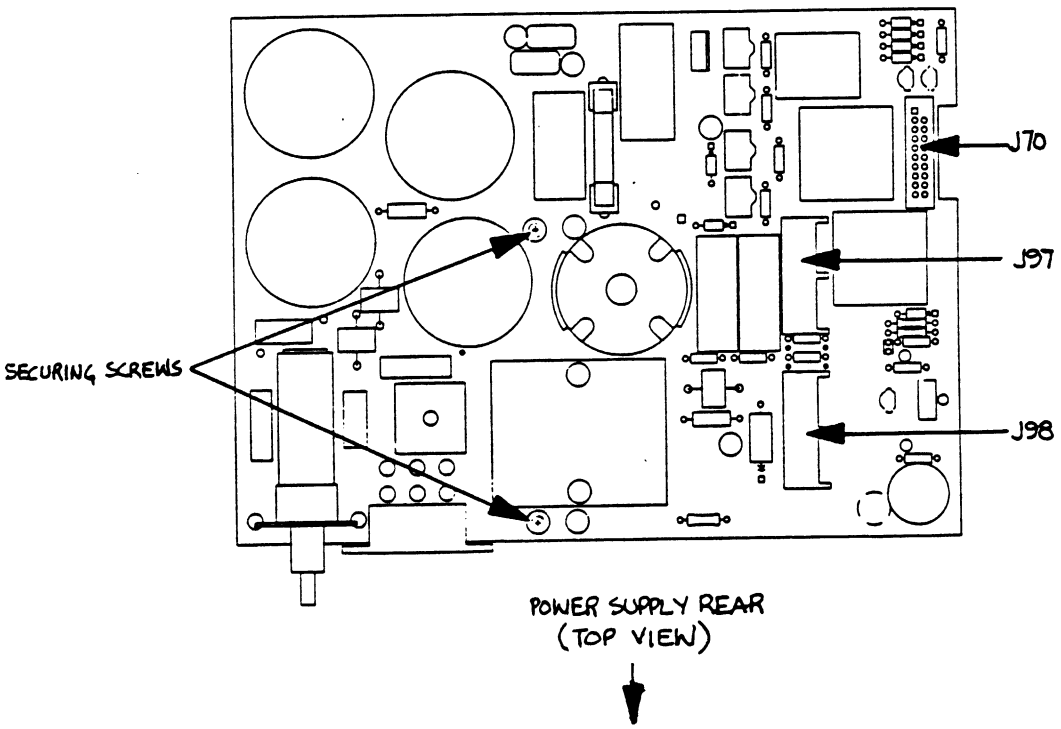


Figure 6100-317. Connector locations for removal of the A2 Line Inverter Board.

4. Remove the two screws from the left side of the power supply rear plate, above and below the power plug receptacle. (See Fig. 6100-318).

   a. Remove the two long screws from the right side of the fan motor housing. (See Fig. 6100-318).

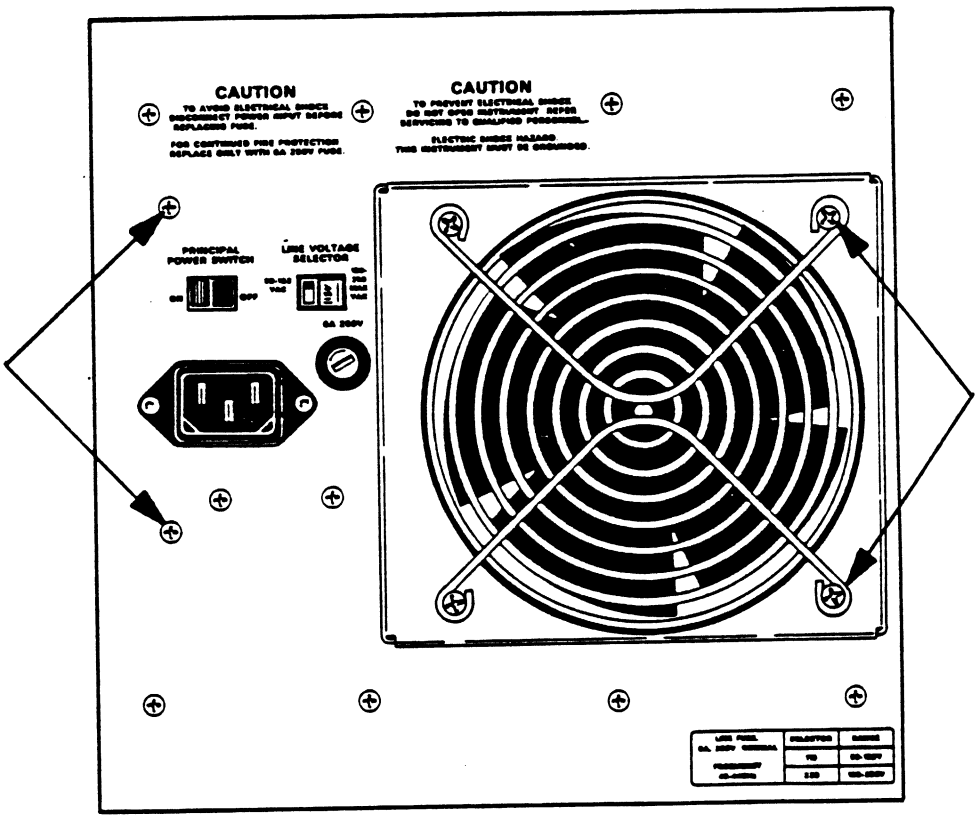


Figure 6100-318. Location of rear panel screws securing the power supply cover.

b. Remove the overall cover from the power supply unit.

5. Remove connector J70 from the right front edge of the A2 Line Inverter Board (see Fig. 6100-307). Gently separate the Line Inverter Board from the A3 Control Rectifier Board. (The interconnecting pins of J97 and J98 hold them together).

6. Unsolder the (white) wire connecting the Line Inverter Board to the line filter at the filter.

- Unsolder the (white) wire connecting the Line Inverter to the fuseholder, at the fuseholder.

NOTE

When removing a wire from a circuit board, always tag the wire and the corresponding connection point on the circuit board.

7. Remove the Line Inverter Board.

8. To replace the A2 Line Inverter Board, reverse the order of removal. Match the index triangle on the pin connectors with the corresponding triangle on the board. Correct location of the pin connectors is shown in the circuit board illustrations.

CAUTION

Check that the circuit board is held in place by its plastic guides on both edges. These guides are mounted inside the overall power supply cover.

A3 Control Rectifier Board

Remove and replace the A3 Control Rectifier Board as follows:

1. Remove the power supply. (See ''Power Supply Removal'', in this section).

2. Remove the protective cover from the power supply. (See ''Access to Components in the Power Supply'', in this section).

3. Follow steps 3 and 4 of the ''A2 Line Inverter Board Removal'' procedure (in this section) to remove the overall cover from the power supply chassis.

4. With reference to Fig. 6100-319, remove connector J70 connector at the upper front edge of the Control Rectifier Board. Remove connector J81 (to the fan motor) which is located near the lower right board.

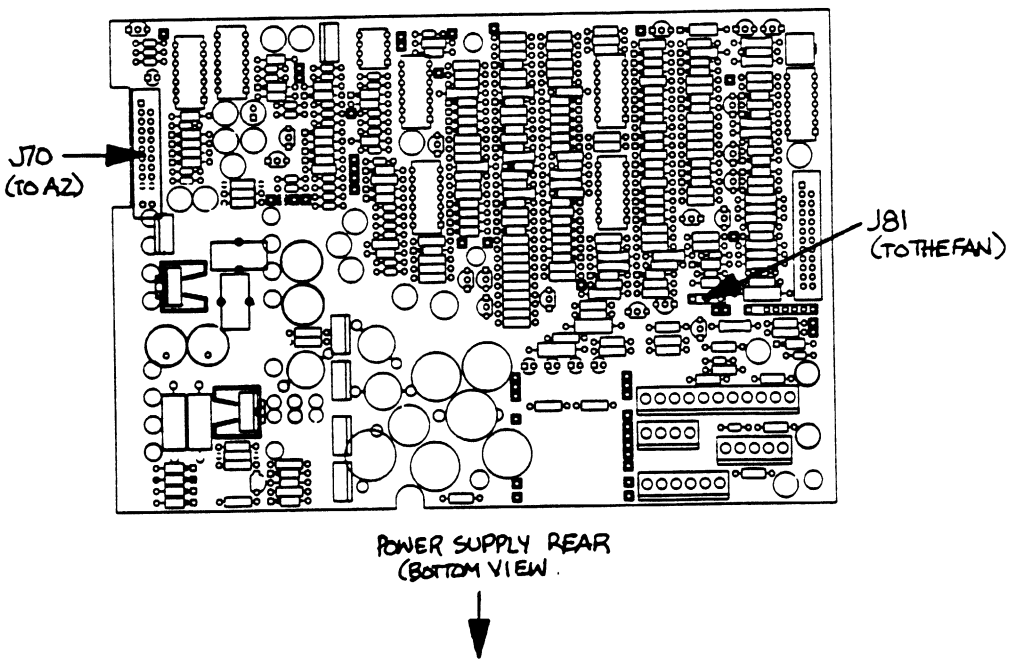


Figure 6100-319. Connector locations for removal of the A3 Control Rectifier Board.

5. Remove the two screws below and to the right of the power plug receptacle on the 11401/11402 rear panel (see Fig. 6100-320). Gently separate the Control Rectifier Board from the A2 Line Inverter Board. The interconnecting pins in J97 and J98, on the A2 Line Inverter Board, hold both boards together (see Fig. 6100-317).

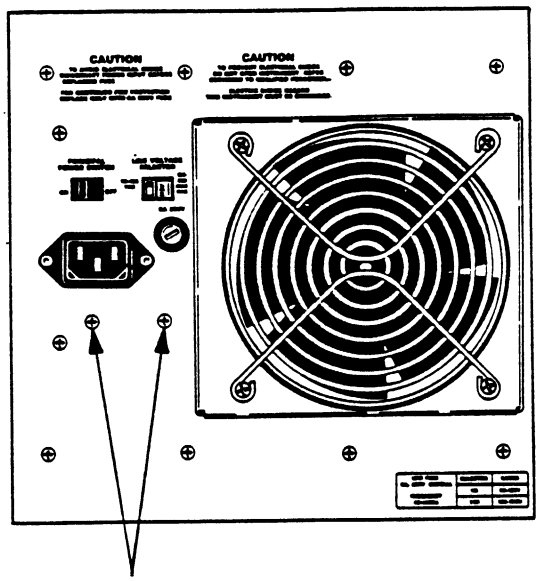


Figure 6100-320. Rear panel mounting screws for the A3 Control Rectifier Board.

6. Remove the Control Rectifier Board.

CAUTION

The A2 Line Inverter Board is now unfastened and requires support so it does not fall and become damaged.

7. To replace the A3 Control Rectifier Board, reverse the order of removal. Match the index triangles on the pin connectors with the corresponding triangles on the board. The correct location of the pin connectors is shown in the circuit board illustrations.

CAUTION

Check that the circuit board is held in place by its plastic guides on both sides. These guides are mounted inside the overall power supply cover.

A4 Regulator Board

Remove and replace the A4 Regulator Board as follows:

1. Remove the power supply. (See ''Power Supply Removal'', in this section).

2. If it is on its side, set the 11401/11402 right side up.

3. Disconnect connectors J57 and J60 from the Regulator Board (see Fig. 6100-321). Note the connector index triangle locations for correct reconnection.

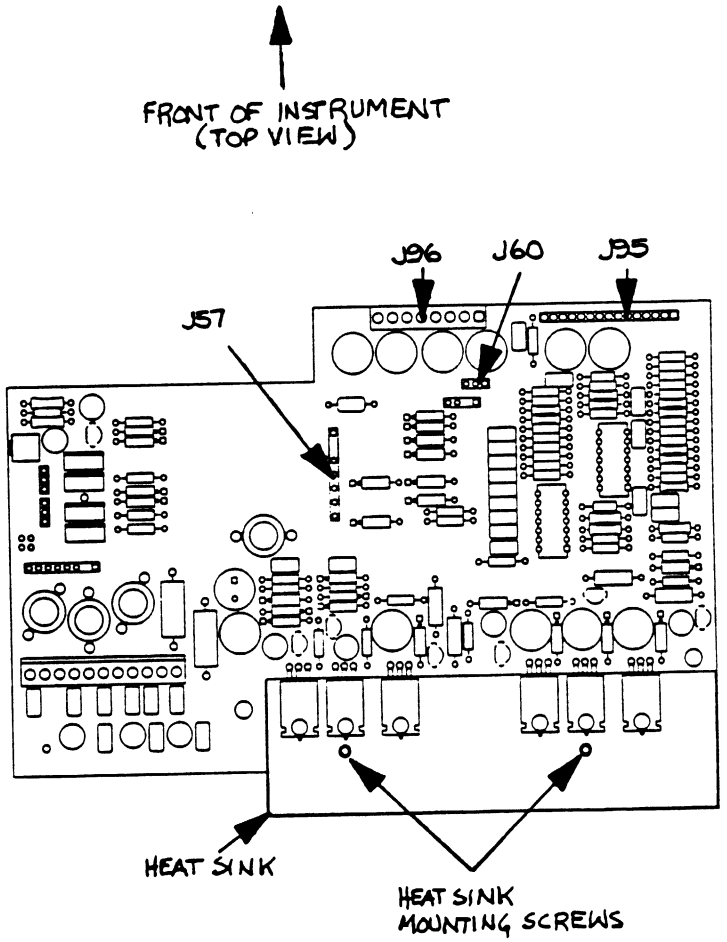


Figure 6100-321. Connector locations for removal of the A4 Regulator Board.

4. Remove the two Torx-head screws from the metal heat-sink attached to the rear of the board (see Fig. 6100-321).

NOTE

The Regulator Board is now unfastened from the chassis. However, it remains connected to the A1 Plug-In Interface Board through interconnecting pins.

5. Carefully disconnect the J95 and J96 pins from the Plug-In Interface Board by pulling the Regulator Board toward the rear.

6. Remove the Regulator Board.

7. To replace the A4 Regulator Board, reverse the order of removal.

CAUTION

Use care when reconnecting the J95 and J96 pins to the A1 Plug-In Interface Board. (Should it become necessary, the A5 Acquisition Board may be removed to view these pins through the mainframe chassis. See the following A5 procedure).

NOTE

Match the index triangle on the pin connectors with the corresponding triangle on the circuit board. Correct locations of the pin connectors are shown in the circuit board illustrations.

A5 Acquisition Board

Remove and replace the A5 Acquisition Board as follows:

1. Turn the instrument on its right side (as viewed facing the front). The board is located beneath the card cage and the power supply compartments and beside the A6 Time Base Board.

2. Remove the eight Torx-head screws from the board. (See Fig. 6100-322).

NOT AVAILABLE AT THIS TIME

Figure 6100-322. Connector locations for removal of the A5 Acquisition Board.

3. Move the rear side of the board outward. Position the board so that its outside edge is about perpendicular to the bottom of the oscilloscope. Do not stress the wire bundles.

NOTE

Record the positions of the connectors and the receptacles to aid in their correct reinstallation.

4. Disconnect the peltola connectors from the center and board edge areas. (See Fig. 6100-322).

5. Disconnect connectors J85, J66B, J91C, J86, J84, and J91A from along the inside edge of the board.

6. Remove the Acquisition Board.

7. To replace the A5 Acquisition Board, reverse the order of removal.

CAUTION

Don't pinch any interconnecting wires underneath the board. Arrange the wires away from the posts to which the Torx-head screws will be fastened.

A6 Time Base Board

Remove and replace the A6 Time Base Board as follows:

1. Turn the instrument on its right side (as viewed facing the front). The board is located next to the CRT bottom and beside the A5 Acquisition Board.

NOTE

Record the positions of each connector to aid in their correct replacement.

2. Remove connector J09 (see Fig. 6100-323).

NOT AVAILABLE AT THIS TIME

Figure 6100-323. Connector locations for removal of the A6 Time Base Board.

3. Remove connectors J85, J66A, J83, J86, J84, and J91.

4. Remove the nine spacer posts from the board.

5. Remove the Time Base Board.

6. To replace the A6 Time Base Board, reverse the order of removal.

CAUTION

The 11401/11402 has static-sensitive components. Be sure to observe all special precautions mentioned under the heading ''Static-Sensitive Device Classification''.

Don't pinch any interconnecting wires.

A7 Display Controller Board

Remove and Replace the A7 Display Controller Board as follows:

1. Remove connectors J57, J53, J52A, and J63C from the board (see Fig. 6100-324). Note the index triangles on each connector so they can be replaced correctly.

2. Remove the six Torx-head screws.

3. Remove the Display Controller Board. Lift and extract the board toward the right side of the 11401/11402 (as viewed facing the front).

   - Notice that the inside edge is held fast by slots in each bottom edge of the circuit board guides. (These guides secure the circuit boards within the card cage compartment).

4. To replace the A7 Display Controller Board, reverse the order of removal.

CAUTION

Observe the routing of wires underneath the board. Do not pinch any interconnecting wires when replacing the board.

NOTE

Insert the inner edge of the board back into each of the slots of the board guides. (Be certain the guides are seated correctly on top of the circuit boards in the card cage).

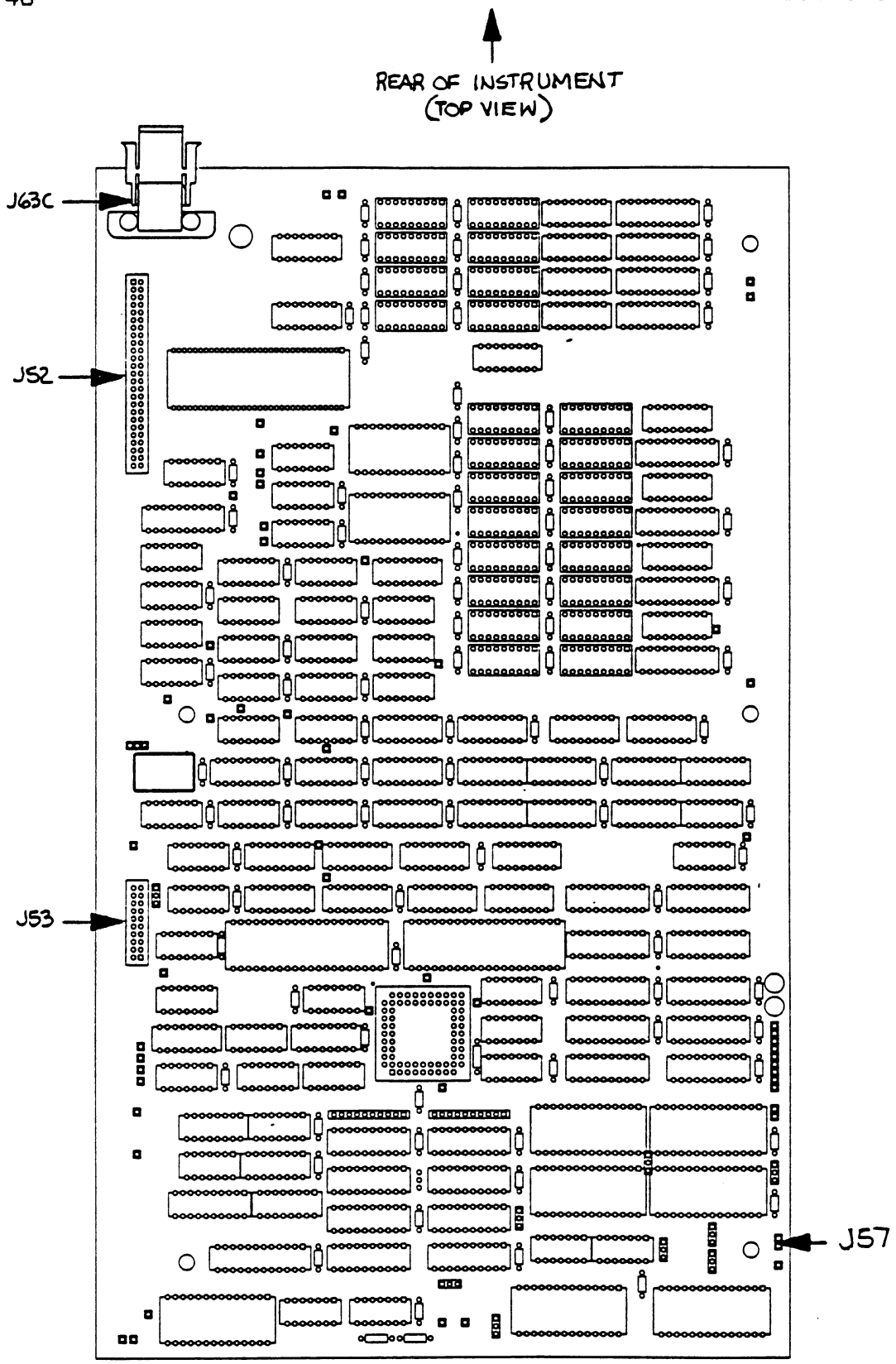


Figure 6100-324. Connector locations for removal of the A7 Display Controller Board.

A8 CRT Driver Board

Remove and replace the A8 CRT Driver Board as follows:

1. Remove the CRT shield and the CRT. (See ''Cathode-Ray Tube Removal'', in this section).

2. Remove connectors J57 and J53 (see Fig. 6100-325). Note the position of connector index triangles so the connectors can be correctly replaced.

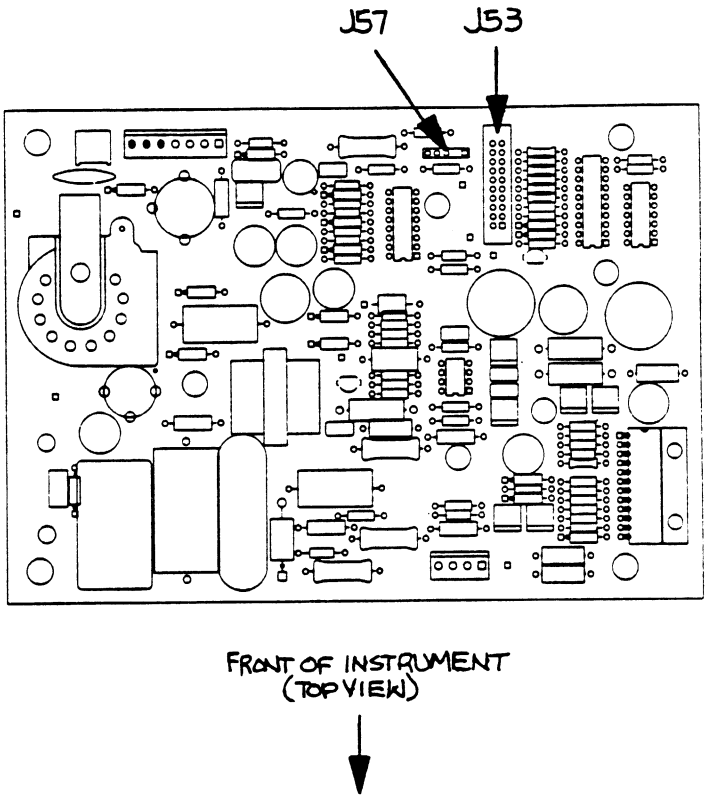


Figure 6100-325. Connector locations for removal of the A8 CRT Driver Board.

3. Remove the Torx-head screws from each corner of the board.

4. Remove the CRT Driver Board by lifting the outside edge of the board.

5. To replace the A8 CRT Driver Board, reverse the order of removal.

A9 Touch Panel Board

Remove and replace the A9 Touch Panel Board as follows:

1. Remove the front-panel bezel. (Refer to ''Cathode-Ray Tube Removal'', in this section). Begin with step 6 and proceed through step 9.

NOTE

The wire cable from P73 on the A10 Front-Panel Control Board may be removed with A9. (See Fig. 6100-327). Disconnect connector P73 from the A10 front-panel control board. Note the position of connector index triangles in order to correctly replace the connector. Carefully remove the wire cable through the slot provided in the front casting.

Protect the front of the bezel while it is removed. Since the plastic exterior may scratch, cover it with protective material.

2. Lay the bezel on its face. Remove the five screws that retain the Touch Panel Board to the bezel.

3. Remove the Touch Panel Board.

NOTE

Check the position of the plastic diffuser inside and under the board. If the Touch Panel Board is replaced, reinstall the diffuser in the same position.

4. To replace the A9 Touch Panel Board, reinstall the board on the bezel.

NOTE

Check that the diffuser is correctly reinstalled.

5. Install the five screws loosely to hold the board. Center the menu buttons through the bezel holes. Tighten the screws.

6. If P73 was removed from the A1Ø Front-Panel Control Board, route the wire cable back through the slot in the chassis. Attach the connector to the board after checking the index triangles for correct orientation.

7. Replace the bezel. (Refer to ''Cathode-Ray Tube Replacement'', in this section). Use steps 4 through 7.

NOTE

Feed any slack cable from P73 to inside the chassis (near the A1Ø Front-Panel Control Board). Be careful not to pinch the interconnecting cable when the bezel is replaced.

A10 Front-Panel Control Board

Remove and replace the A10 Front-Panel Control Board as follows:

1. Remove the crt shield. (See ''Cathode-Ray Tube Removal'', in this section). Follow steps 1 and 2.

2. Remove connector J53 from the A7 Display Controller Board. (See Fig. 6100-324).

3. Remove connectors P72, P75, P73 and P74. (See Fig. 6100-327). Note the position of their index triangles for correct replacement.

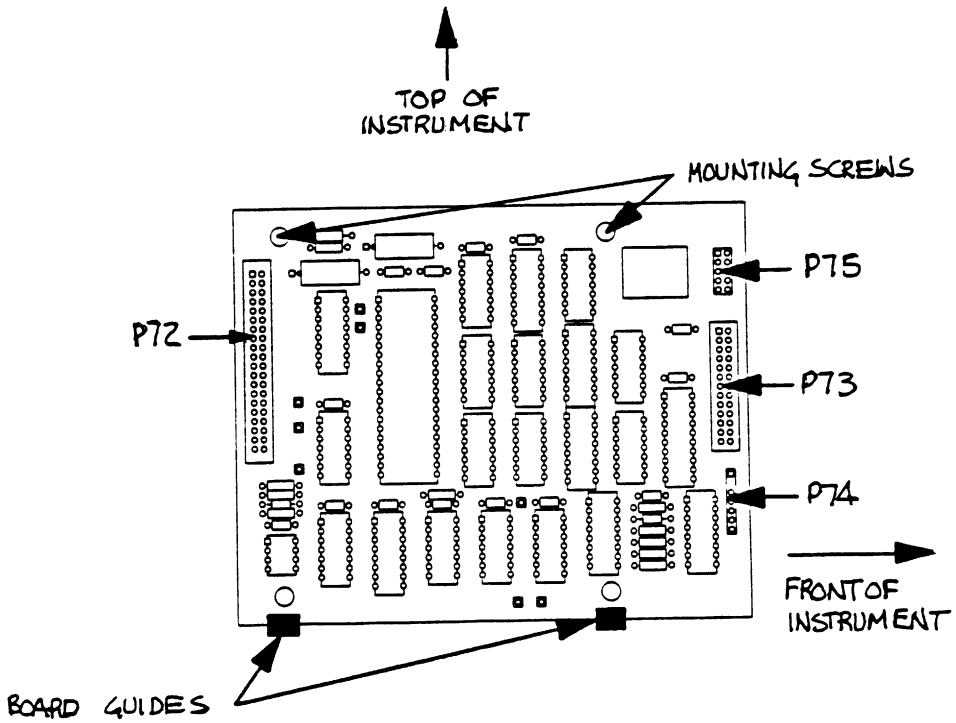


Figure 6100-327. Connector locations for removal of the A10 Front Panel Control Board.

4. Remove the two Torx-head screws at the upper edge of the board. (See Fig. 6100-327).

5. Lift the board away from the guides at its bottom and remove it.

6. To replace the A10 Front-Panel Control Board, reverse the order of removal.

A11 Front-Panel Button Board

Remove and replace the A11 Front-Panel Button Board as follows:

1. Remove the A7 Display Controller Board. (See ''A7 Display Controller Board'', in this section).

2. Remove the crt shield. (See ''Cathode-Ray Tube Removal'', in this section). Follow steps 1 and 2.

3. Remove connector P75 from the A10 Front-Panel Control Board (see Fig. 6100-327). Note the position of connector index triangles for correct replacement.

4. Remove the two Torx-head screws from the Front-Panel Button Board, which is located at the top and near the inside center of the front casting.

5. Remove the Front-Panel Button Board.

6. To replace the A11 Front-Panel Button Board, reverse the order of removal.

A12 Rear Panel Board

Remove and replace the A12 Rear Panel Board as follows:

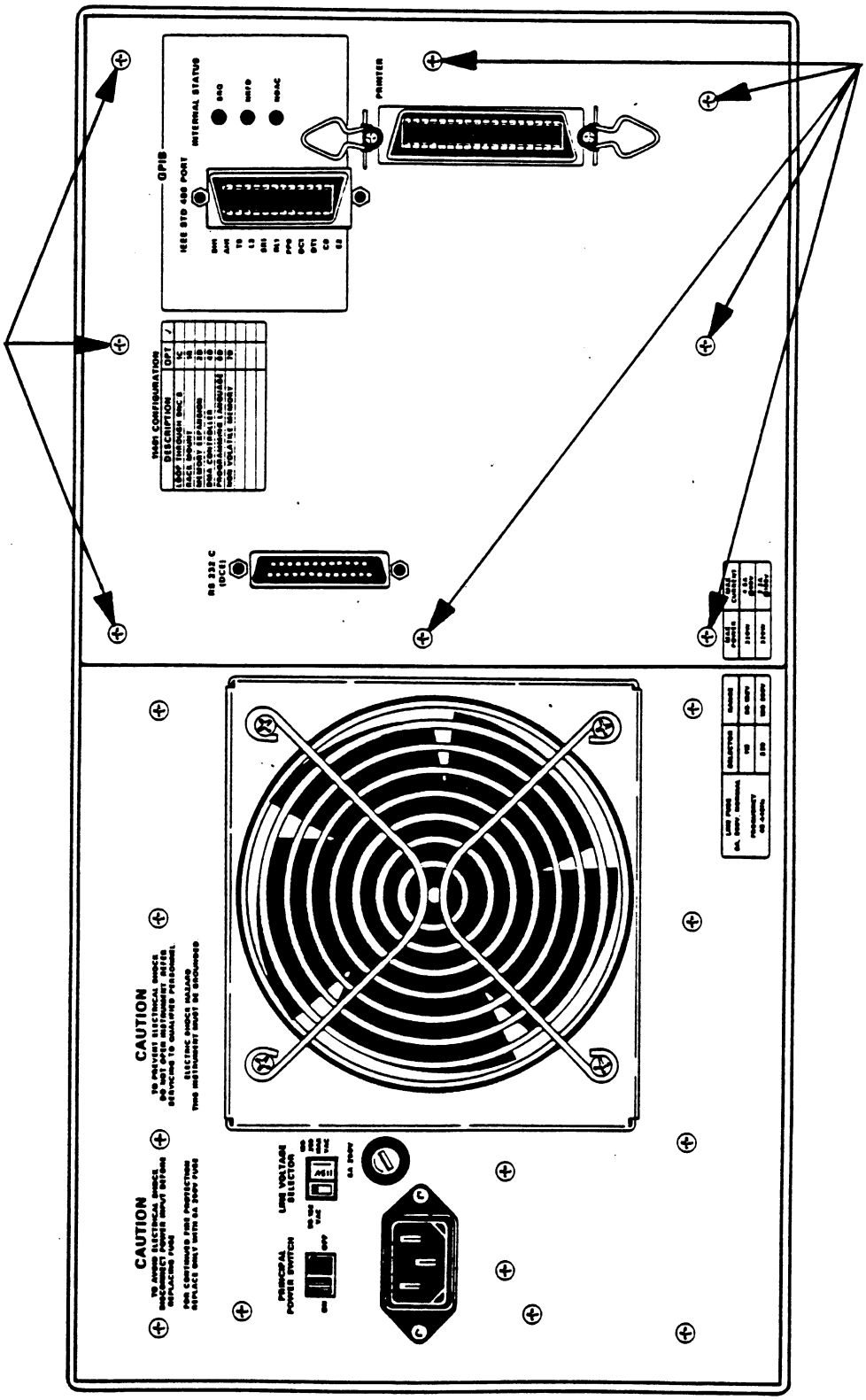


Figure 6100-329. Location of rear mounting screws.

1. Remove the eight Torx-head screws from the outer edges of the rear panel plate. (See Fig. 6100-329).

2. Tilt the plate back from the mainframe. Remove connector J78 from the top of the A12 Rear Panel Board. Note the position of connector index triangles for correct replacement.

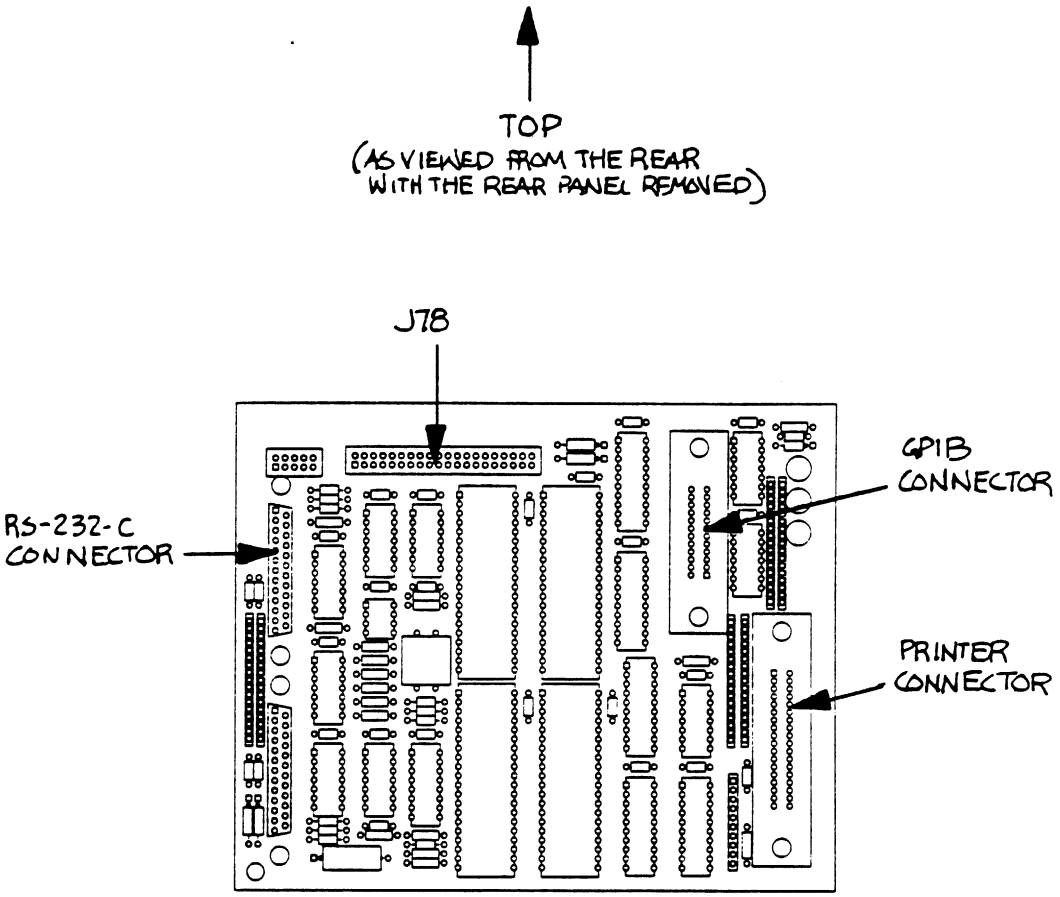


Figure 6100-330. Connector locations for removal of the A12 Rear Panel Board.

3. Remove the rear panel plate and its attached A12 Rear Panel Board.

4. Remove the following items from the rear panel plate.

   - Torx-head screw and washer (at lower left, if present),
   - Two retainers, screws, and washers from the Printer connector,

- Two screws from the GPIB connector, and
- Screws, lockwashers, and flat washers from the RS-232-C connector(s).

5. Remove the Rear Panel Board from the plate.

CAUTION

The metal covers on the Printer and on the GPIB connectors are loose. If the board is inverted, they will fall off.

6. To replace the A12 Rear Panel Board, reverse the order of removal.

NOTE

Replacement of connector J78 will be easier if the connector is replaced before the plate is reinstalled.

A13 Mother Board

Remove and replace the A13 Mother Board as follows:

1. Remove both circuit board guides from atop the card cage. The guides are retained by two small catches, located in two holes in the left side bracket of the card cage. The other ends of the guides contain slots which attach to the edge of the A7 Display Controller Board. Both ends of the guides can be pried loose for removal.

2. Remove the A14 I/O, A15 MMU, A16 Compressor, A17 Main Processor, and A18 Memory Circuit Boards. (See ''Plug-On Boards'', in this section).

NOTE

Tag the interconnecting plugs and mark the board locations so that they can be replaced correctly.

3. Remove connector J63B from the Mother Board.

4. Remove the six Torx-head screws.

5. Remove the Mother Board.

6. To replace the A13 Mother Board, reverse the order of removal.

NOTE

Don't pinch the wires along the inside edge of the board when replacing it.

Plug-On Boards

All circuit boards inside the card cage plug onto the A13 Mother Board. Feed-through connectors join the plug-on boards to the Mother Board. Figure 6100-331 shows the location of each board within the card cage.

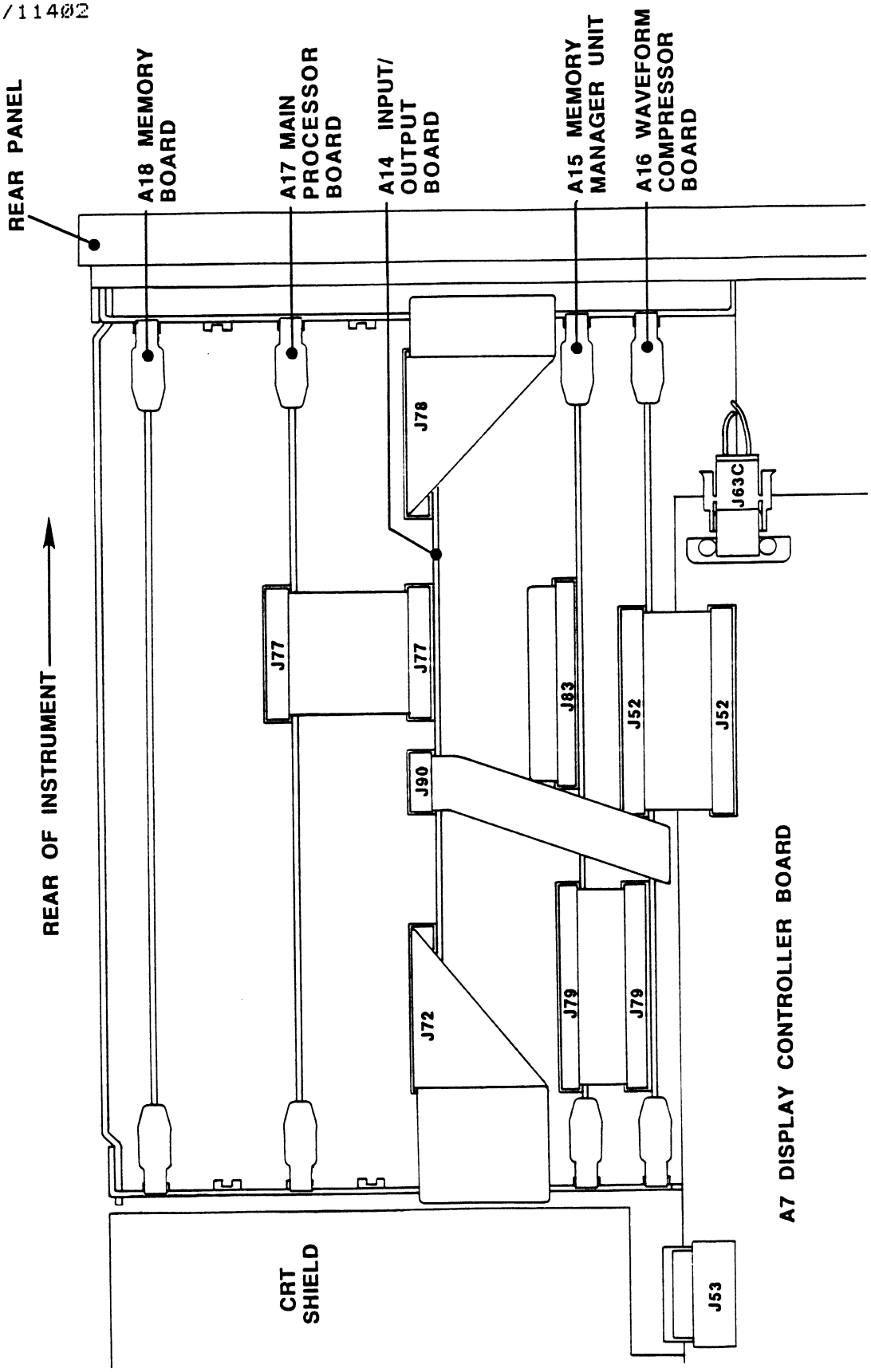


Figure 6100-331. Top View of card cage showing circuit board locations.

A14 Input/Output Board

Remove and replace the A14 I/O Board as follows:

1. Remove both circuit board guides from atop the card cage. These guides are retained by two small catches located in two holes in the left bracket of the card cage. The other ends of the guides contain slots which attach to the edge of the A7 Display Controller Board. Both ends of the guides can be pried loose for removal.

2. Remove connectors J78, J77, J90 and J72. Note the position of connector triangles for correct replacement. (See Fig. 6100-331 for the location of A14 in the card cage and Fig. 6100-332 for connector locations).

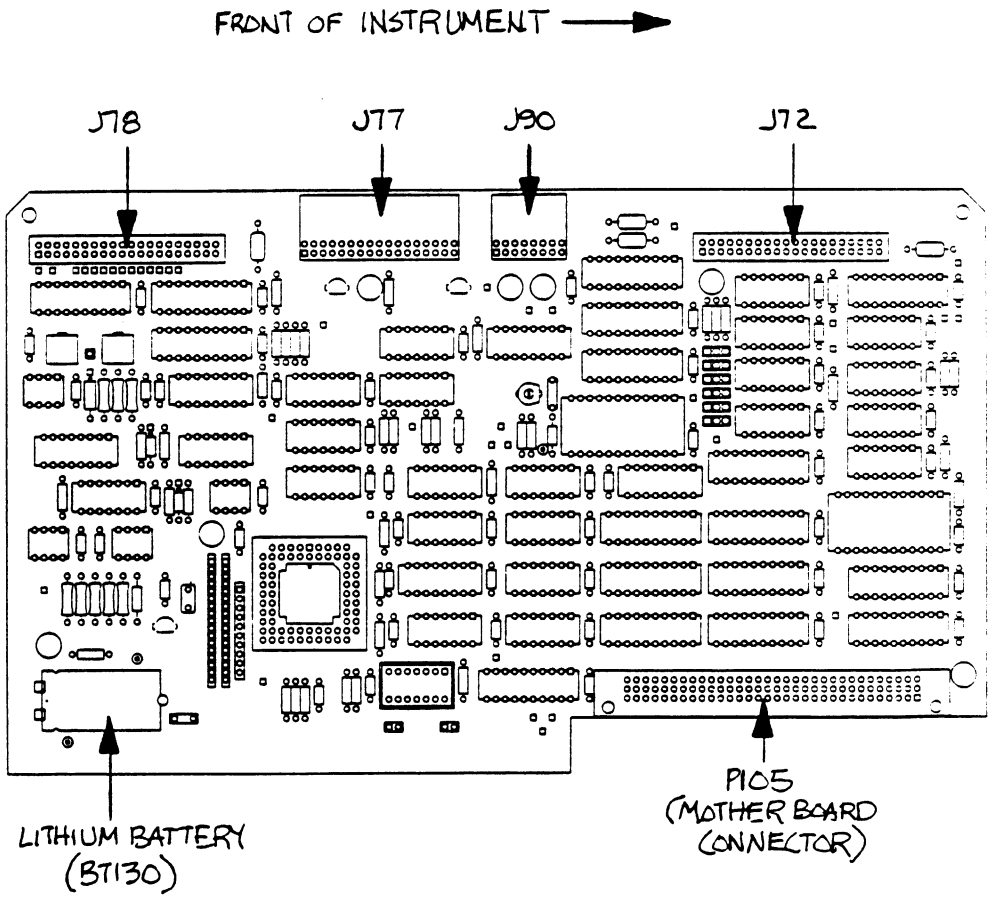


Figure 6100-332. Connector locations for removal of th A14 Input/Output Board.

3. Lift the white, hinged tab at the upper front edge of the board. Pull the tab upward until the I/O Board separates from the Mother Board.

4. Remove the I/O Board.

WARNING

A lithium battery (BP130) is mounted on the I/O Board. ***This battery requires special handling for disposal.*** *Read the instructions on* ***"Lithium Battery Handling and Disposal"****, in this section.*

5. Replace the A14 I/O Board by reversing the order of removal.

NOTE

Insert the board edges into the plastic guides at each end of the card cage. Lower the board into position.

Check that connector P105 is seated on the Mother Board connector (see Fig. 6100-331). Push down firmly on the I/O Board to connect it.

A15 Memory Manager Unit (MMU) Board

Remove and replace the A15 MMU Board as follows:

1. Remove both circuit board guides from atop the card cage. The guides are retained by two small catches located in two holes in the left bracket of the card cage. The other ends of the guides contain slots which attach to the edge of the A7 Display Controller Board. Both ends of the guides can be pried loose for removal.

2. Remove connectors J83 and J79. (See Fig. 6100-331 and 6100-333). Note the position of connector index triangles for correct replacement.

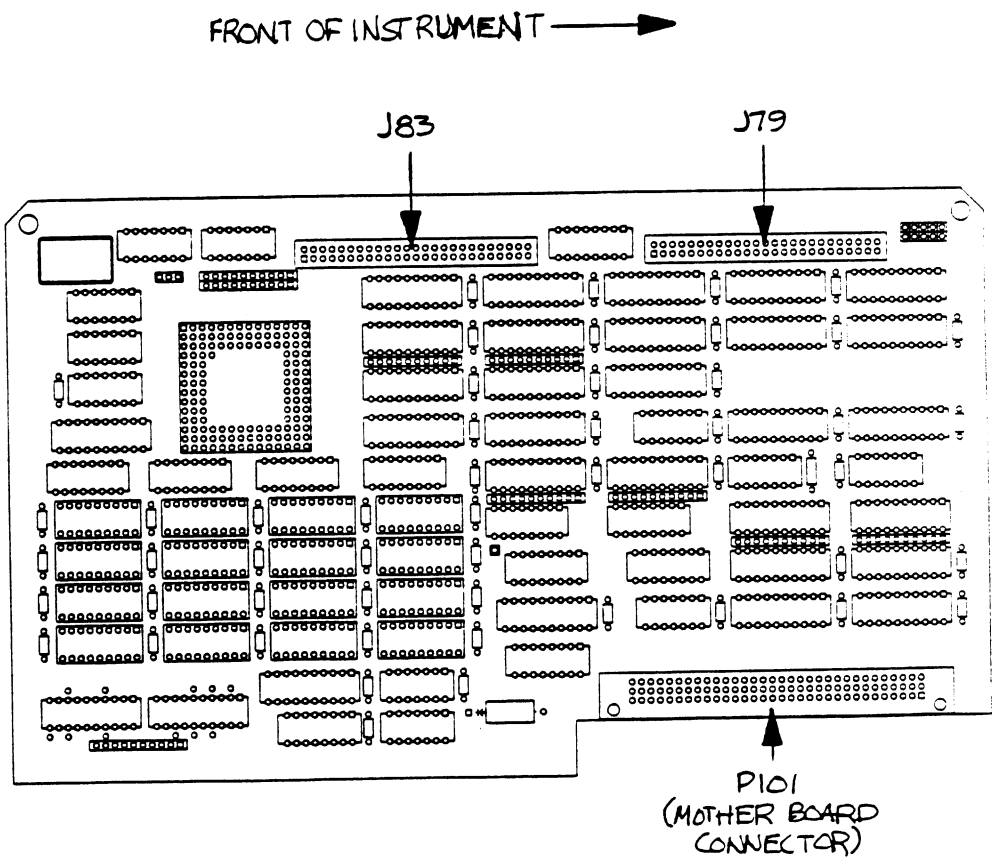


Figure 6100-333. Connector locations for removal of the A15 Memory Manager Unit Board.

3. Remove J90 from the A14 I/O Board.

4. Lift the white, hinged tabs at the front and rear edges of the board. Pull the tabs upward until the MMU Board separates from the Mother Board.

5. Remove the MMU Board.

6. Replace the A15 MMU board by reversing the order of removal.

NOTE

Insert the board edges into the plastic guides at each end of the card cage. Lower the board into position.

Check that connector P101 is seated onto the Mother Board connector. Push down firmly on the MMU Board to connect it.

A16 Waveform Compressor Board

Remove and replace the A16 Waveform Compressor Board as follows:

1. Remove both circuit board guides from atop the card cage. The guides are retained by two small catches located in two holes of the left bracket of the card cage. The other ends of the guides contain slots which attach to the edge of the A7 Display Controller Board. Both ends of the guides can be pried loose for removal.

2. Remove connectors J52 and J79. (See Fig. 6100-331 and 6100-334). Note the position of connector index triangles for correct connector replacement.

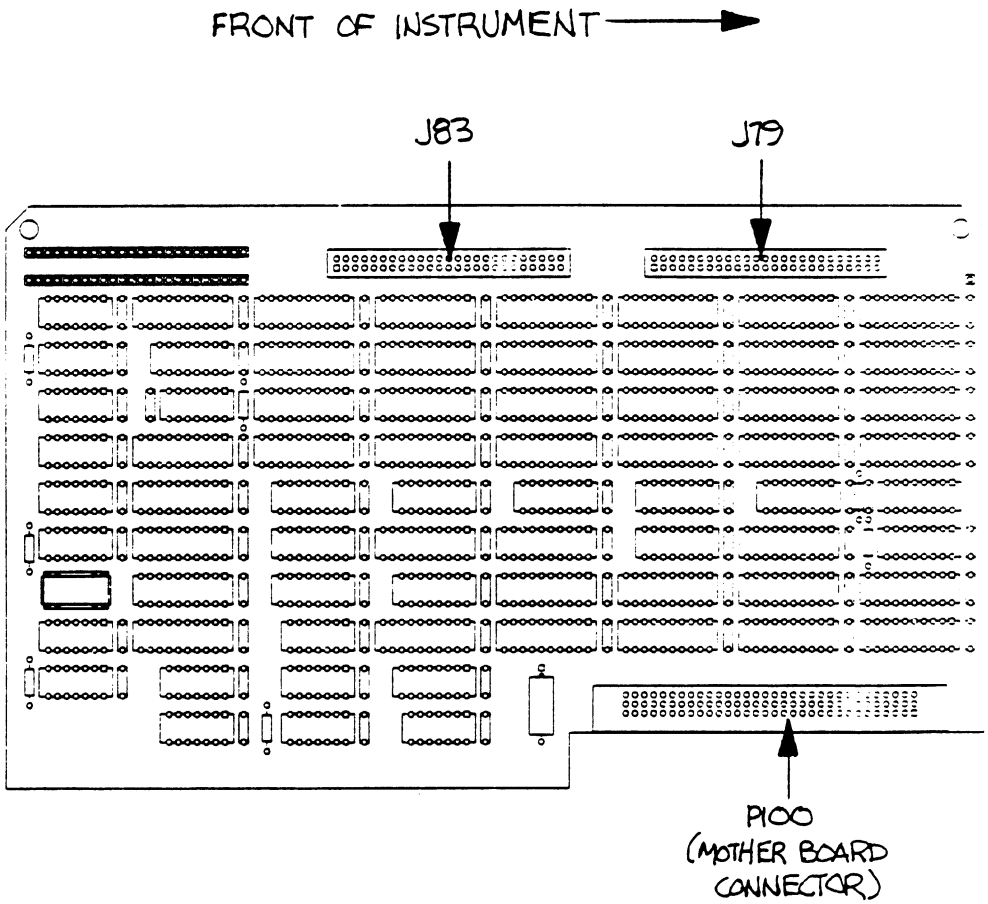


Figure 6100-334. Connector locations for removal of the A16 Waveform Compressor Board.

3. Remove J90 from the A14 I/O Board. (See Fig. 6100-332).

4. Lift the white, hinged tabs at the front and rear edges of the board. Pull the tabs upward until the Waveform Compressor Board separates from the Mother Board.

5. Remove the Waveform Compressor Board.

6. Replace the A16 Waveform Compressor Board by reversing the order of removal.

NOTE

Insert the board edges into the plastic guides at each end of the card cage. Lower the board into position.

Check that connector P100 is seated onto the Mother Board connector. Push down firmly on the Waveform Compressor Board to connect it.

A17 Main Processor Board

Remove and replace the A17 Main Processor Board as follows:

1. Remove both circuit board guides from atop the card cage. The guides are retained by two small catches located in two holes in the left bracket of the card cage. The other ends of the guides contain slots which attach to the edge of the A7 Display Controller Board. Both ends of the guides can be pried loose for removal.

2. Remove connector J77. (See Fig. 6100-331 and 6100-335).

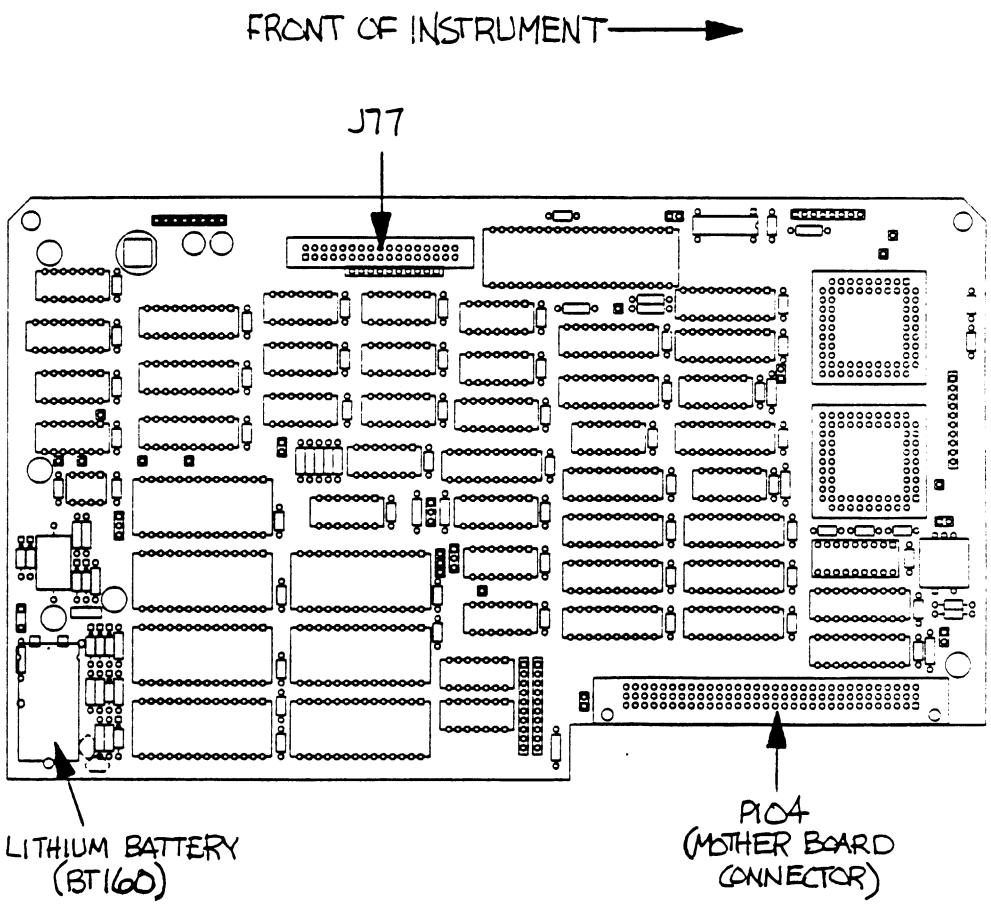


Figure 6100-335. Connector locations for removal of the A17 Main Processor Board.

3. Lift the white, hinged tabs at the front and rear edges of the board. Pull the tabs upward until the Main Processor Board separates from the Mother Board.

4. Remove the Main Processor Board.

WARNING

A Lithium battery (BT160) is mounted on the Main Processor Board. ***The battery requires special handling for disposal.*** *Read the instructions on the* ***"Lithium Battery Handling and Disposal"****, in this section.*

5. Replace the A17 Main Processor Board by reversing the order of removal.

NOTE

Insert the board edges into the plastic guides at each end of the card cage. Lower the board into position.

Check that connector P104 is seated onto the Mother Board connector. Push down firmly on the Main Processor Board to connect it.

A18 Memory Board

Remove and replace the A18 Memory Board as follows:

1. Remove both circuit board guides from atop the card cage. The guides are retained by two small catches located in two holes in the left bracket of the card cage. The other ends of the guides contain slots which attach to the edge of the A7 Display Controller Board. Both ends of the guides can be pried loose for removal.

2. Lift the white, hinged tabs at the front and rear edges of the board. Pull the tabs upward until the Memory Board separates from the Mother Board. (See Fig. 6100-331 for the location of A18 within the card cage).

3. Remove the Memory Board.

4. Replace the A18 Memory Board by reversing the order of removal.

NOTE

Insert the edges of the board into the plastic guides at each end of the card cage. Lower the board into position.

Check that connector P106 is seated onto the Mother Board connector. Push down firmly on the Memory Board to connect it.

Front-Panel Bezel Removal

To remove and replace components inside the Front-Panel Bezel, proceed as follows:

1. Remove the bezel. Refer to "Cathode-Ray Tube Removal", in this section and follow steps 6 through 10.

2. Disconnect connector P73 from the A10 Front-Panel Control Board (See Fig. 6100-327). Remove the wire cable through the slot in the front casting.

3. Remove the bezel and set it aside.

4. To replace the front-panel bezel, refer to "Cathode-Ray Tube Replacement", in this section and follow steps 4 through 7.

S74 and S75 Encoder Removal

To remove and replace the S74 and S75 Encoder, proceed as follows:

1. Remove the front-panel bezel and the crt. (Refer to "Cathode Ray Tube Removal", in this section).

2. Remove the plastic shaft extender by pulling it off.

3. Remove the 7/16" nut and the washer.

4. Remove the encoder(s) from the casting by pulling toward the interior of the instrument. (Notice the way its key fits into the casting keyway).

5. Unsolder the wires from the encoder(s).

NOTE

When removing wires from a component, record their locations for replacement.

6. Remove the Encoder(s).

   - Connector P74 can be disconnected (from the A10 Front-Panel Control Board) if both encoders are removed.

7. To replace the S74 or S75 Encoder, reverse the order of removal. For the crt, refer to the "Cathode Ray Tube Replacement" procedure.

NOTE

Be certain that the wires are correctly replaced on the encoder(s).

Align the key on the Encoder(s) with the keyway(s) in the front casting before tightening the nut.

If it was removed, replace connector P74 on the A10 Front-Panel Control Board.

Rear Panel

To remove the Rear Panel, proceed as follows:

1. Remove the Rear Panel plate and board. (Refer to the A12 Rear Panel Board removal procedure, in this section). Follow steps 1 through 5.

   - The Rear Panel board is now accessible for troubleshooting and/or repair.

CAUTION

The metal covers on the Printer and on the GPIB connectors are loose. They will fall off if the board is inverted.

2. To replace the Rear Panel, reverse the order of removal.

Semiconductors

Semiconductors should not be replaced unless actually defective. If removed from their sockets during routine maintenance, return them to their original sockets. Unnecessary replacement of semiconductors may affect the adjustment of the instrument. When semiconductors are replaced, check the operation of circuits that may be affected.

WARNING

To avoid an electric-shock hazard, always disconnect the instrument from its power source before removing or replacing components.

Replacement semiconductors should be of the original type or a direct replacement. The lead configurations of semiconductors used in this instrument are shown in Figure 6100-339. Some plastic-case transistors have lead configurations which differ from those shown. If a replacement transistor is made by a different manufacturer than the original, check the manufacturer's basing diagram for correct basing. All transistor sockets in this instrument are wired for standard basing as used for metal-cased transistors. When removing soldered-on transistors or integrated circuits, use an anti-static vacuum solder extractor (see Soldering Techniques procedure in this section) to remove the solder from the circuit board pads. Transistors which have heat radiators or are mounted on the chassis use silicone grease to increase heat transfer. Replace the silicone grease on both sides of the insulating washer when replacing these transistors.

WARNING

Handle silicone grease with care. Avoid getting the silicone grease in your eyes. Wash hands thoroughly after use.

NOT AVAILABLE AT THIS TIME

Figure 6100-339. Semiconductor lead configurations.

To replace one of the power transistors mounted on the metal heat-sink at the rear of the power supply (A4 Regulator board), first remove the board. (See the A4 Regulator Board Removal procedure in this section). Then unsolder the transistor leads, remove the mounting screw from its heat radiator, and remove the transistor and its insulating washer. When replacing the transistor, be sure to reinstall the insulating washer between the transistor and the heat sink (use silicone grease as previously described). Reinstall the mounting screw and tighten it just enough to hold the transistor in place. Then solder the replacement transistor to the A4 Regulator Board. Replace the board by reversing the order of removal.

An extracting tool should be used to remove in-line integrated circuits to prevent damaging the pins. This tool is available from Tektronix, Inc.; order Tektronix Part 003-0619-00. If an extracting tool is not available, use care to avoid damaging the pins. Pull slowly and evenly on both ends of the integrated circuit. Try to avoid disengaging one end from the socket before the other end. **(Most ICs will be soldered into the circuit board, rather than in sockets).**

CAUTION

Do not remove stickers affixed to the top of EPROMs. Removing such stickers will admit light into the chip, and may cause partial erasure of its data.

Hypcon Connectors

The **hypcon** (**hy**brid-**p**rinted **con**nector) is a precision-made connector designed to provide low loss electrical and thermally efficient connection between the printed circuit board and hybrid integrated circuits. An exploded view of the hypcon connector is shown in Figure 6100-340. When replacing the hybrid IC's, be careful not to touch the elastomer gold-plated contacts with your fingers, or to use a cleaner which will degrade contact reliability. **If it becomes necessary to use a cleaning solvent near the connector when replacing adjacent (within 1/2") circuit board components, the hypcon connector and hybrid IC should be removed.**

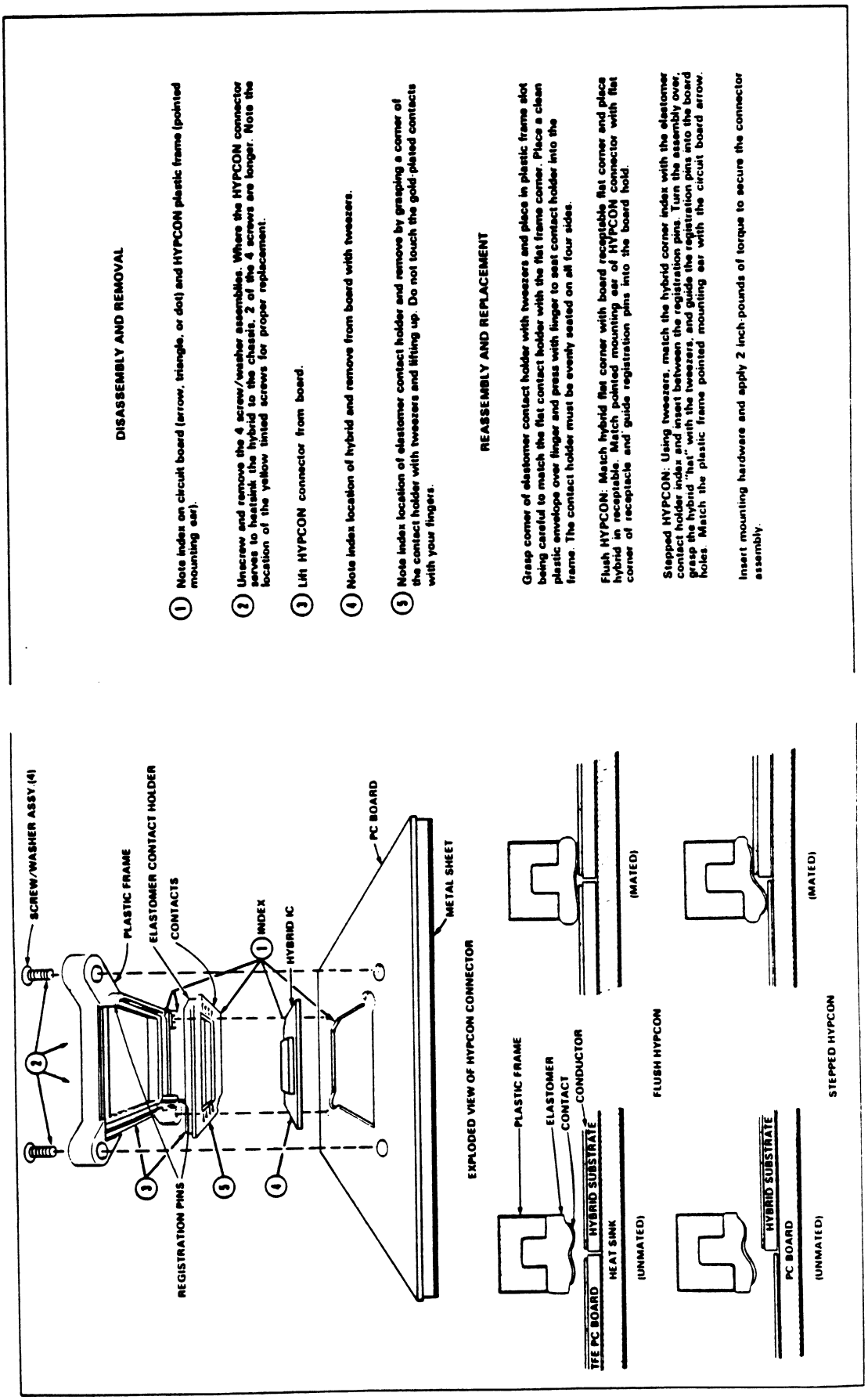


Figure 6100-340. HYPCON assembly removal and replacement.

IMPORTANT: Remove all traces of solder flux or foreign material contamination from the circuit board contact area before replacing the connector. **Contamination usually takes place during the soldering and cleaning process.** Even when the soldering is done carefully, flux, oil, or other contaminants can be carried under the connector during the cleaning operation. When the solvent evaporates, nonconductive contaminants may remain on or near the contact interfaces.

The cleaning process (either hand cleaning with a solvent or machine cleaning in an automatic detergent wash) is **not** recommended for boards containing hypcon connectors.

If a component near a hypcon connector must be replaced, the following steps are recommended:

1. Remove the hybrid IC and hypcon connector (see Disassembly and Removal Instructions) before any soldering or cleaning and store in a dirt-free covered container. When several hybrids and hypcon connectors are to be removed, keep parts together and replace as sets; do not interchange parts.

2. Hand Soldering:

   a. Use small diameter solder (Ø.ØЗØ inch-Ø.Ø4Ø inch).

   b. Use low wattage soldering irons (15-2Ø watts).

   c. Use care with solder and placement.

3. Remove solder flux and contact contamination with isopropyl alcohol, denatured ethyl alcohol, or a FREON TF cleaner such as SPRAY-ON #2ØØ2.

4. Flush the hybrid and Hypcon connector mounting area with isopropyl alcohol. Do not scrub with a cotton-tipped applicator, as cotton fibers will adhere to edges and surfaces of contact area and cause open or intermittent connections. The elastomer should be examined under light for dust, hair, etc., before it is reinstalled. If the etched circuit board surfaces require more cleaning, scrub with a soft rubber eraser and blow or vacuum clean while dusting the surface with a small clean brush.

5. If the hybrid IC and elastomer contact holder are contaminated, clean by flushing or spraying with alcohol and oven dry at 50° C. Do not scrub with a cotton-tipped applicator or similar device. If the contact holder is excessively contaminated, replace it with a new one.

Tighten the hypcon mounting screws to two inch-pounds of torque.

Make sure that the elastomer is properly seated in the contact holder before remounting the assembly to the circuit board. Exercise care when mounting the frame--elastomer contact holder--hybrid IC assembly to the circuit board to prevent misalignment between the connector and board.

CAUTION

Because of the close tolerances involved, special care must be taken to ensure correct index alignment of each hypcon part during reassembly. Failure to do so can crack the hybrid substrate. (See Figure 6100-340 for index locations).

If your instrument contains both the flush and stepped type of hypcon connectors, be careful not to mix the elastomer contact holders during reassembly. Flush hypcon connectors have green elastomer contact holders and the plastic frame is marked FLUSH. Stepped hypcons have neutral-colored elastomer contact holders with a slight ridge or step on the contact surface, the large frames are marked STEPPED. The registration pins on the stepped plastic frame are slightly longer than those on the flush frame. The elastomer contact holder in the small stepped connectors is indexed differently than the large connectors. Look for a small gold arrow in one corner of the holder instead of a flat corner. Match this corner arrow with the pointed corner of the plastic frame. Give close attention to this indexing, because elastomer contact holders can easily be inserted incorrectly.

Differences also exist between the large flush and the large stepped hypcon circuit board receptacles. Figure 6100-340 shows the cross-sectional differences which must be observed when working with an instrument that contains both types of hypcon connectors.

CAUTION

Damage to the elastomer contact holder can result if the connectors are not mated properly with the board receptacle.

When replacing the hybrid, insert it into the board opening and then position the hypcon connector in the board registration holes for perfect alignment. The outer portion of the hypcon frame should be flush with the circuit board before the four mounting screws are tightened. Avoid touching the hybrid and elastomer contact with your fingers; finger oils can degrade reliability.

A procedure for removal and replacement is included in Figure 6100-340.

Hybrid Integrated Circuits

The A5 Acquisition Board has a Hybrid IC (U1710).

The IC is mounted to the inside of its heatsink cover. The cover is orientated to the circuit board in two ways. First, two of the socket screws are offset. This allows the cover to be reinstalled only one way. Second, one corner is flat rather than rounded as are the other corners. This flat corner matches an etched design on the board.

To remove a Hybrid IC, proceed as follows:

1. Remove the four 1/4" retaining nuts from the heatsink cover.

2. Lift the cover (and the IC) from its socket.

CAUTION

Avoid touching the IC or the socket contacts with your fingers. Finger oils can degrade reliability.

Replace the Hybrid IC as follows:

1. Orient the replacement IC to fit the socket. Align the flat corner of the cover to the flat corner etched design on the circuit board.

2. Press the IC toward the board to feel the spring tension of the contacts. **Move the cover around until the IC seats flush against its sockets.**

3. Hold the IC in place and install the four retaining nuts. Tighten them **fingertight.**

4. Use a torque wrench to tighten the nuts in a **diagonal method only** to 3 1/2 to 4" pounds.

CAUTION

Do not tighten these nuts clockwise.
That will crack the heatsink cover.

*Instead, **use this diagonal method** to tighten them. Begin at the lower right nut and tighten it. Go diagonally across the cover to the upper left nut Tighten it. Next, drop down to the lower left nut and tighten it. Then, go diagonally across the cover to the upper right nut. Tighten it.*

Diagonally check that all four nuts are tightened to the recommended torque. (See step 4).

Microcircuit Integrated Circuits

There are two microcircuit ICs on the A5 Acquisition Board. They are the U1200 and U1220 Interpolators.

These microcircuit ICs have integral heatsinks. The IC is orientated to the circuit board in two ways. First, three locator posts (inside the cover) bracket the IC. Two posts are at one end and the third at the other end. Second, the cover has a flat-edged corner which matches with an etched design on the board.

To remove the Microcircuit IC, proceed as follows:

1. Remove the four 1/4" retaining nuts from the cover.

2. Lift the IC (and attached cover) from its socket.

CAUTION

Avoid touching the IC or the socket contacts with your fingers. Finger oils can degrade reliability.

Replace the Microcircuit IC as follows:

1. Align the flat edge corner of the cover with the matching design on the board. This orients the IC correctly.

2. Check that the locator pins fit in their respective locations.

3. Press the IC toward the board to feel the spring tension of the contacts.

4. Hold the IC in place and install the four retaining nuts. Tighten them **finger tight.**

5. **Tighten the nuts using a diagonal method only.** See the following warning for diagonal tightening instructions.

    a. Use a torque wrench to tighten the nuts to 3 1/2 to 4" pounds.

CAUTION

Do not tighten these nuts clockwise. *That will crack the heatsink cover. Use a diagonal nut tightening procedure. See the Hybrid Integrated Circuit replacement procedure, immediately preceding this part.*

Chip Carrier "Slam-Pack" Integrated Circuits

Several circuit boards have these ICs. They include the A5 Acquisition Board, the A6 Time Base Board, the A7 Display Controller Board, the A14 Input/Output Board, the A17 Main Processor Board, and the A18 Memory Board.

Some Chip Carrier ICs have raised, ridged heatsink covers. Others have flat covers. The IC is oriented to its socket by a flat corner. The other corners are notched to fit the edges of the socket. The flat-edged corner of the IC aligns with a "spring" (small metal tab) at one corner of the socket.

To remove a Chip Carrier IC, proceed as follows:

1. Hold the cover in place, unfasten the holding clip by pushing it aside. It may help to push down slightly on the cover.

2. Remove the cover slowly to prevent the IC from falling out.

NOTE

Observe the index of the IC before removing it.

3. Remove the IC with tweezers.

CAUTION

Avoid touching the IC or the socket contacts with your fingers. Finger oils can degrade reliability.

Replace the Chip Carrier IC as follows:

1. Using tweezers, put the flat edge of the replacement IC against its index spring.

CAUTION

Check that the spring in the corner does not get bent by the flat corner index, which may short the corner two contacts.

2. Arrange the other corners with tweezers to fit evenly at the edges of the socket.

3. Set the cover flat on the chip with the end tabs properly aligned with the mating recesses in the socket.

4. Push down on the cover, keeping it flat on the chip, and slide the cover into place. Hold it there while moving the holding clip over the tabs on the opposite end of the cover.

5. Check that the cover is secure.

Interconnecting Pins

Two methods of interconnection are used to electrically connect circuit boards with other boards and components. When the interconnection is made with a coaxial cable, a special end-lead connector plugs into a socket on the board. Other interconnections are made with a pin soldered into the board. Two types of connectors are used for these interconnecting pins. If the connector is mounted on a plug-on board, a special socket is soldered into the board. If the connector is on the end of a lead, an end-lead pin connector is used which mates with the interconnecting pin. The following information provides the removal and replacement procedure for the various types of interconnecting methods.

Coaxial-type End-lead Connectors (Peltolas)

The last number (of Jxxx) indicates the color, or the color stripe, of the wire insulation.

Replacement of coaxial-type end-lead connectors requires special tools and techniques. Only experienced maintenance personnel should attempty to remove or replace these connectors. We recommend that the damaged cable or wiring harness be replaced as a unit. For cable or wiring harness part numbers, see the Replaceable Mechanical Parts List. An alternative solution is to refer the replacement of the defective connector to your local Tektronix Field Office or representative. Figure 6100-341 gives an exploded view of a coaxial end-lead connector assembly.

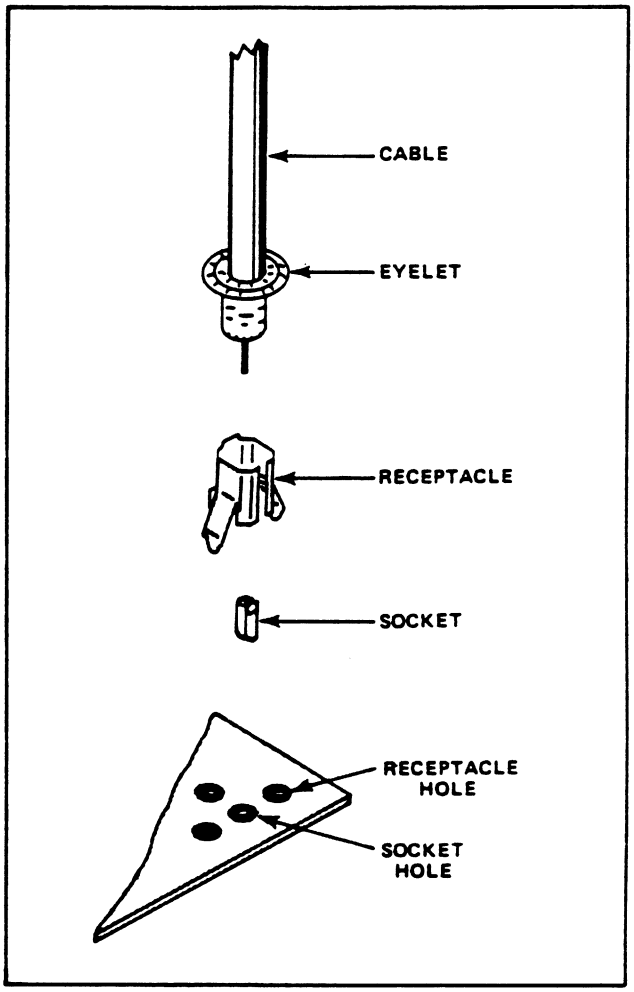


Figure 6100-341. Coaxial end-lead connector assembly.

Circuit-Board Pins

Replacing circuit-board pins on multi-layer boards is not recommended. (All circuit boards in the 1140i are multi-layer boards.)

Circuit-Board Pin Sockets

The pin sockets on the circuit boards are soldered to the back of the board. To remove or replace one of these sockets, first unsolder the pin (use an anti-static vacuum-type desoldering tool to remove excess solder). Then straighten the tabs on the socket and remove the socket from the board. Place the new socket in the circuit board hole and press the tabs down against the board. Solder the tabs of the socket to the circuit board; be careful not to get solder inside the socket.

CAUTION

The spring tension of the pin sockets ensures a good connection between the circuit board and the pin. This spring tension can be destroyed by using the pin sockets as a connecting point for spring-loaded probe tips, alligator clips, etc.

Multi-Pin Connectors

The pin connectors used to connect the wires to the interconnecting pins are clamped to the ends of the associated leads. To remove or replace damaged multi-pin connectors, remove the old pin connector from the end of the lead and clamp the replacement connector to the lead.

Some of the pin connectors are grouped together and mounted in a plastic holder. The overall result is that these connectors are removed and installed as a multi-pin connector. If the individual end-lead pin connectors are removed from the plastic holder, note the order of the individual wires for correct replacement into the holder.

Arrangement of Pins in Multi-Pin Connectors

Pin 1 on multi-pin connectors is designated with a triangle (or arrowhead). A triangle, dot, or square printed on circuit boards denotes pin 1. When a connection is made to a circuit board, the orientation of the triangle on the multi-pin holder is determined by the index (triangle, dot or square) printed on the circuit board. (See Fig. 6100-343). Most circuit-board mounted connectors have a triangle index mark.

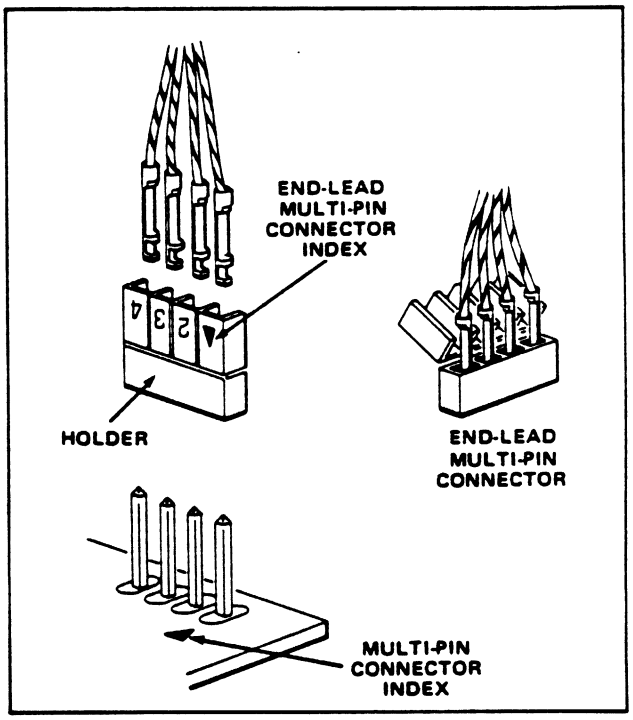


Figure 6100-343. Orientation of multi-pin connectors.

NOTE

Some multi-pin connectors are keyed by a gap between the pin 1 and 3 positions in the holder. (A small plastic plug covers the pin 2 position on the end of the holder). There is a corresponding gap between pins 1 and 3 on the circuit board.

Align the gap in the multi-pin holder with the gap between the circuit board pins. The connector is then ready to be installed.

Many of the larger, gray-colored, multi-pin ribbon connectors have a red line along one side of their attached wire cables. This red line indicates the location of pin 1 and 2 or the location of the triangle index mark.

Some of the gray-colored ribbon cables may have the number of their connectors stamped on them.

The ribbon connectors have two functions. The first is to provide a strain release for the wire connections. The wire ribbon is wrapped around a bar in between the wire connections and the top of the connector. Strain is then felt between the wires and the top of the connector. This releases most of the strain which would otherwise be felt on the wire connections.

The second function on most of the ribbon connectors is to provide a pull-tab to ease disconnection. A white-colored pull-tab is attached inside the connector. When the tab is pulled, even pressure is applied across the connector. The connector separates from its holder easily.

NOTE

To remove these gray-colored ribbon connectors, grasp the white pull-tab (fastened into the connector, if there) and pull it loose from the holder.

If there isn't a white pull tab present in the connector, grasp the ends of the connector instead. Pull it straight out from the connector socket.

If a ribbon connector is found with an open or shorted wire, individual wires cannot be removed or replaced. The ribbon connector and cable must be replaced.

Plug-in Interface Connectors

Individual contacts of plug-in interface connectors can be replaced. If several contacts are damaged, we recommend replacing the entire A1 Plug-In Interface Board. An alternate solution is to have your local Tektronix Field Office repair or replace the damaged A1 Plug-In Interface board.

Use the following procedure to remove and replace an individual contact of the plug-in interface connectors:

1. Remove the A1 Plug-In Interface Board as previously described. (Refer to the A1 Plug-In Interface Board Removal procedure in this section.)

2. Snap the white plastic connector cover off the side of the damaged plug-in interface connector.

3. Unsolder and remove the damaged contact.

NOTE

Don't melt the connector with the soldering iron while unsoldering or soldering the contact.

4. Install the replacement contact. Carefully position it to fit against the connector body. Re-solder the new contact.

5. Snap the white plastic connector cover back onto the plug-in interface connector. Check that the replaced contact is aligned with the other contacts.

6. Replace the A1 Plug-In Interface Board by reversing its order of removal.

Power Transformer

Replace the power transformer only with a direct replacement Tektronix transformer. Remove and replace the power transformer as follows:

1. Remove the A3 Control Rectifier Circuit Board as described under Circuit Board Removal in this section. (See Figure 6100-344).

NOT AVAILABLE AT THIS TIME

Figure 6100-344. Location of the power transformer on the A3 Control Rectifier Board.

NOTE

Record the position of the transformer leads so they may be correctly replaced.

2. Unsolder the transformer leads from the A3 Control Rectifier Board. Remove any excess solder from the circuit-board pads (see Soldering Techniques, in this section).

3. Remove the transformer.

4. Place the new transformer in position and solder the leads to the A3 Control Rectifier circuit-board pads.

5. Replace the A3 Control Rectifier in the power supply as described under Circuit Board Removal in this section.

NOTE

Refer to the "Adjustment After Repair" procedure, at the end of this section.

Line Fuse

The Line fuse used in the 11401/11402 is located on the rear panel of the power supply. Replace the line fuse (F99) with one of proper type and rating.

NOTE

Line voltage fuse F99 is used for both 110- and 220-volt operation. No change in the fuse is necessary when switching the LINE VOLTAGE SELECTOR switch between 110 volts and 220 volts.

Adjustment After Repair

After any electrical component has been replaced, the adjustment of that particular circuit should be checked, as well as the adjustment of any closely related circuits. Because the low-voltage supplies affect all circuits, adjustment of the entire instrument should be checked if component replacements have been made in these supplies or if the power transformer has been replaced.

(SEE TABLE 1 ON FOLLOWING PAGE.)

Part 5
Diagnostics

Preliminary

Diagnostics

Board Swap Guide

This section correlates all possible error codes resulting from Diagnostic tests with the primary and secondary board(s) suspected of causing each error. The primary suspect board should be inspected for loose connections or components then, if the Diagnostic errors are repeated, it should be replaced with a known good board. Make sure that the new board is configured exactly like the old one and that any installed firmware matches the version in the old board. In addition, refer to Table 1, Adjustments Required after Circuit Board or Module Replacement, in Section 4, Corrective Maintenance, for necessary adjustments and any precautions.

Diagnostics are composed of two stages. The first are the Kernel Diagnostics that verify the subsystem processors and their associated hardware such as ROM, RAM and control signals. After all Kernel tests have passed without failure the second stage tests, called Self Tests, will run. They verify the remainder of the instrument circuitry. The Extended Diagnostics are a superset of the instrument Self Tests that run at power-up. Any Self Test fault will cause the instrument to enter Extended Diagnostics. Circuits that are not fully tested are listed in this section under Circuits Not Covered by Diagnostics.

The error codes and tests are divided into three groups based on the three mainframe processors: Executive/Main, Display, and Digitizer. The prefix letters on the error codes, E, D, and G refer to these processors, respectively. These groups are also used in the Diagnostic Error Code Listings in this part of the document. Each processor group has a table of Kernel Diagnostic error codes and a table of Extended Diagnostic error codes.

Error codes listed with "manual" in parentheses indicate tests that are manually performed and that produce no error code displays. They are included to help you locate faulty boards. Interconnections, such as mother boards and cables, and the power supply boards are not listed but should always be considered as problem sources.

Extended Diagnostics (Self-Tests)

After all Extended Diagnostic tests have run any resultant error codes appear on the display next to the associated circuit block names in the Extended Diagnostics menu. Each circuit block that had a failure will give the first error encountered and the number failures in the block. Select the label of a failed block then select the Area label to get a more complete list of the error codes in a block. Selecting the Routine label shows the lowest level test routines in the selected Area. The currently selected Block, Area, and Routine are shown below their labels at the bottom of the menu. Several operating mode selectors are also available at the bottom of the screen. When certain test routines are selected some of these operating modes may become unselectable. The mode operators are:

(E)Exit—Extended Diagnostics is terminated and the instrument enters the normal operating mode.

(p)Loop—Toggles On and Off. When On, the selected test(s) is run continuously with the number of iterations displayed.

(t)Terse—Toggles On and Off. When On, tests in the loop mode run at the fastest rate but the iteration readout is not updated until the test is stopped (by touching the screen or a button).

(x)All—Toggles On and Off. When On, all tests in the current menu are selected to run when started.

(s)Stop of Err—Toggles On and Off. When On, testing stops after the first failed test completes.

(r)Run/(q)Quit—Starts or stops the currently selected tests.

Touching any place on the screen (or any front panel button) while a test is running will stop the test when the current routine ends.

Kernel Diagnostics

The Kernel Diagnostic tests run concurrently in all three subsystem processor circuits at power-up. Address, data, and control lines to local ROM (containing the kernel test code) and RAM and the interrupt controllers are all verified. For the Executive/Main Processor, this means checking basic operation for most boards in the Executive card cage (i.e., those plugged in to the motherboard). The last test for each processor is to verify communication with the other processors. All Kernel tests must run without failures before the Self Tests will start.

Each processor kernel produces error codes that are read in different ways. In most cases the error codes are read as binary bits then converted to hexadecimal numbers. The method for reading the error codes is described under each processor's table of error codes under Diagnostic Error Code Listing in this part of the document. Each Kernel table below gives suspect boards for one processor's Kernel error codes.

Abbreviations of Board Names

All active mainframe boards are listed here with the abbreviation used in the board-swap tables below. Non-active boards such as the Executive mother board and connecting cables are not included in this list.

ACQ	Acquisition Board	(A5)
TB	Time Base Board	(A6)
DSY	Display Controller Board	(A7)
CRT	CRT	(V70)
CRTDR	CRT Driver Board	(A8)
TOUCH	Touch Panel Board	(A9)
FPCTRL	Front Panel Control Board	(A10)
FPBUT	Front Panel Button Board	(A11)
REAR	Rear Panel Board	(A12)
IO	I/O Board	(A14)
MMU	MMU Board	(A15)
CMPR	Compressor Board	(A16)
MPU	Main Processor Board	(A17)
MEM	Memory Board	(A18)

Executive/Main Processor Error Codes

TABLE
Main Processor Kernel Error Codes

Error Index	Primary Suspect	Secondary Suspects
1F—14	MEM	MPU
13—11	IO	MPU
10—0F	MPU	IO
0E	FPCTRL	IO, MPU
0D—0C	IO	MPU
0B—09	REAR	IO, MPU
08—06	MMU	MPU
05	MPU	MEM
04	user selected RS232 external loopback test	

TABLE
Executive/Main Processor Extended Error Codes

Error Index	Primary Suspect	Secondary Suspects
E111X—E112X	MPU	
E113X—E11AX	MEM	MPU
E121X—E122X	MPU	
E123X—E12AX	MEM	MPU
E13XX	MEM	MPU
E14XX	MEM	MPU
E15XX	MPU	
E16XX	MPU	
E17XX	IO	MPU
E18XX	IO	MPU
E191X	MPU	
E192X	MPU	IO
E193X	MPU	IO
E194X	MPU	IO
E1AXX	MEM	MPU
E1BXX	MPU	
E1CXX	MPU	MEM
E21XX	FPCTRL	IO, MPU
E22XX	FPCTRL	TOUCH, IO, MPU
E23XX	FPCTRL	TOUCH, IO, MPU
E24XX	FPCTRL	IO, MPU
E251X (manual)	FPBUT	FPCTRL, TOUCH, IO, MPU
E252X (manual)	TOUCH	FPCTRL, IO, MPU
E253X (manual)	FPCTRL	IO, MPU
E3XXX	IO	MPU
E4XXX	REAR	IO, MPU
E51XX	MMU	MPU
E52XX	MMU	MPU
E53XX	CMPR	MPU
E54XX	CMPR	MPU
E55XX	CMPR	MPU
E561X	DSY	CMPR, MMU, MPU
E562X	TB	MMU, MPU
E57XX	IO	MPU
E581X	LEFT	IO, MPU
E582X	CENTER	IO, MPU
E583X	RIGHT	IO, MPU

Display Processor Error Codes

TABLE
Display Processor Kernel Error Codes

Error Index	Primary Suspect	Secondary Suspects
F4	DSY	CMPR
All Others	DSY	

TABLE
Display Processor Extended Error Codes

Error Index	Primary Suspect	Secondary Suspects
D1611	DSY	CMPR
D1631	DSY	CMPR
D1641	DSY	CMPR
D2711 (manual)	CRTDR	DSY, CRT
All Others	DSY	

Digitizer Processor Error Codes

TABLE
Digitizer Processor Kernel Error Codes

Error Index	Primary Suspect	Secondary Suspects
16	TB	MMU
All Others	TB	

TABLE
Digitizer Processor Extended Error Codes

Error Index	Primary Suspect	Secondary Suspects
G11XX—G15XX	TB	
G16XX	TB	MMU
G21XX	ACQ	TB
G22XX—G235X	TB	
G236X	TB	ACQ
G31XX—G32XX	TB	
G33XX	TB	ACQ
G34XX (manual)	ACQ	TB
G35XX—G36XX	ACQ	TB
G41XX—G421X	TB	ACQ
G511X—G52XX	TB	
G53XX	TB	MMU

Diagnostic Error Codes Listing

This section provides listings in numerical order of all test error codes generated by Kernel or Extended Diagnostic tests.

The Extended Diagnostic menu and the failure error codes appear on the screen after all tests have run. Beside each circuit block name will be the first error code encountered and the number of faults in that circuit block. Selecting the label of a failed block then the Area label will give you a more complete list of error codes in a block. Selecting the Routine label shows the lowest level routines in the selected Area.

The Kernel Diagnostic error codes are read in different ways depending on the processor kernel in question. The method used to read the error code for each processor kernel follows its Table of error codes below. In most cases, Kernel error codes are derived by reading binary bits posted by a kernel processor and converting them to a two digit hexadecimal number. The error code indicates the first test that failed. Noting the test that passed before the failure can help to isolate the problem. To aid in troubleshooting, the failed test continues to run in a loop until manually stopped.

These test and error code listings are divided into three groups based on the three mainframe processors: Executive/Main Processor, Display Processor, and Digitizer Processor. This grouping is also used in the Board Swap Guide in the Diagnostics section of this manual. Refer to the Board Swap Guide for further information on Kernel and Extended Diagnostic test operation.

Tests listed without error codes do not yield error codes when run. Plug-in unit error codes are not shown here, but in the appropriate plug-in unit service manual.

Executive/Main Processor

TABLE
Executive/Main Processor Kernel Error Codes

Test Name	Error Code
DRAM Data Lines	(1F)
DRAM Byte Access	(1E)
DRAM Address/Data	(1D)
Bank Select & Memory Configuration	(1C)
ROM U240 Location	(1B)
ROM U240 Checksum	(1A)
ROM U250 Location	(19)
ROM U250 Checksum	(18)
EPROM U630 Location	(17)
EPROM U630 Checksum	(16)
EPROM U730 Location	(15)
EPROM U730 Checksum	(14)
Timer 0 Interrupt	(13)
Timer 1 Interrupt	(12)
Timer 2 Interrupt	(11)
80287 Math Coprocessor	(10)
DMA Controller Interrupt	(0F)
Front Panel Controller Interrupt	(0E)
Serial Data Interface Interrupt	(0D)
Real Time Clock Interrupt	(0C)
GPIB Controller Interrupt	(0B)
Printer Controller Interrupt	(0A)
Std RS232 Controller Interrupt	(09)
MMU Display Talk Request Interrupt	(08)
MMU SAG Interrupt	(07)
MMU RAG Interrupt	(06)
DMA 0 Transfer	(05)
Std RS232 External Loopback (forced by I/O Bd. straps)	(04)

Bit patterns for the above hexadecimal error codes are displayed with the front-panel MENUS LEDs in bottom-to-top bit order. The UTILITY label represents the MSB (most significant bit) and the WAVEFORM label represents the LSB (least significant bit). When lit the LEDs represent a one.

For example: Error code 12*hex* would cause the UTILITY and TRIGGER LEDs to be lit.

The Main Processor error bits can also be read from the Main Processor board (A17) test points TP201 (MSB) to TP205 (LSB). The bits are high (+5 V) true.

TABLE
Executive/Main Processor Extended Error Codes

Block, Area, Error Code or Routine Name	Schematic Number(s)	Board Number(s)
Exec Control (E1XXX)		
ROM Location (E11XX)		
U250 (E111X)	24	A17
U240 (E112X)	24	A17
U630 (E113X)	24	A18
U730 (E114X)	24	A18
U600 (E115X)	24	A18
U700 (E116X)	24	A18
U612 (E117X)	24	A18
U712 (E118X)	24	A18
U620 (E119X)	24	A18
U720 (E11AX)	25	A18
ROM Checksum (E12XX)		
U250 (E121X)	24	A17
U240 (E122X)	24	A17
U630 (E123X)	25	A18
U730 (E124X)	25	A18
U600 (E125X)	25	A18
U700 (E126X)	25	A18
U612 (E127X)	25	A18
U712 (E128X)	25	A18
U620 (E129X)	25	A18
U720 (E12AX)	25	A18
RAM Refresh (E13XX)		
Rate (E131X)	26	A18
Dynamic RAM (E14XX)		
Config (E141X)	26	A18
Data Lines (E142X)	26	A18
Address/Data (E143X)	26	A18
NVRAM (E15XX)		
Battery (E151X)	24	A17
Data Lines (E152X)	24	A17
Address/Data (E153X)	24	A17
Intrrpt Ctrl (E16XX)		
Master (E161X)	24	A17
Slave 1 (E162X)	24	A17
Slave 3 (E163X)	24	A17
Timers (E17XX)		
Timer 0 (E171X)	21	A14
Timer 1 (E172X)	21	A14
Timer 2 (E173X)	21	A14
Diagn Signal (E174X)	21	A14
TimerIntrpts (E18XX)		
Timer 0 (E181X)	21	A14
Timer 1 (E182X)	21	A14
Timer 2 (E183X)	21	A14
MPU Waits (E19XX)		

Display Processor

TABLE
Display Processor Kernel Error Codes

Test Name	Error Code
Static RAM Data Lines	(FF)
Static RAM Address/Data	(FE)
ROM U612 Location	(FD)
ROM U602 Location	(FC)
ROM U612 Checksum	(FB)
ROM U602 Checksum	(FA)
CPU Timer 0	(F9)
CPU Timer 1	(F8)
CPU Timer 2	(F7)
CPU DMA 0	(F6)
CPU DMA 1	(F5)
Executive Communication	(F4)

The name of the first Display kernel test that fails is displayed on the screen. The Display Processor error-code can be read from the Display Controller board (A7) test points labeled 0 (MSB) to 7 (LSB) next to the ST0 and ST1 LEDs. The bits are high (+5 V) true.

TABLE
Display Processor Extended Error Codes

Block, Area, Error Code or Routine Name	Schematic Number(s)	Board Number(s)
Dsy Control (D1XXX)		
ROM Location (D11XX)		
U612 (D111X)	33	A7
U602 (D112X)	33	A7
ROM Checksum (D12XX)		
U612 (D121X)	33	A7
U602 (D122X)	33	A7
Static RAM (D13XX)		
Data Lines (D131X)	33	A7
Address/Data (D132X)	33	A7
Timers (D14XX)		
Timer 0 (D141X)	34,37	A7
Timer 1 (D142X)	34,37	A7
Timer 2 (D143X)	34,37	A7
DMAs (D15XX)		
DMA 0 (D151X)	33,37	A7
DMA 1 (D152X)	33,37	A7
Exec Intrfce (D16XX)		
Command Port (D161X)	37	A7
DMA Access (D162X)	37	A7
Wavefrm Port (D163X)	37	A7
Attributes (D164X)	37	A7

Digitizer Processor

TABLE
Digitizer Processor Kernel Error Codes

Test Name	Error Code
MPU RAM Data Lines	(1F)
MPU RAM Address/Data	(1E)
ROM U281 Location	(1D)
ROM U283 Location	(1C)
ROM U281 Checksum	(1B)
ROM U283 Checksum	(1A)
MPU DMA 0	(19)
MPU DMA 1	(18)
MPU Timer 2	(17)
Executive Communication	(16)

The error code bits of the first Digitizer kernel test that fails can be read from the Time Base board (A6) test connector J290, pins 2 (MSB) to 7 (LSB). The bits are high (+5 V) true.

TABLE
Digitizer Processor Extended Error Codes

Block, Area, Error Code or Routine Name	Schematic Number(s)	Board Number(s)
Dig Control (G1XXX)		
ROM Location (G11XX)		
U281 (G111X)	16	A6
U283 (G112X)	16	A6
ROM Checksum (G12XX)		
U281 (G121X)	16	A6
U283 (G122X)	16	A6
Static RAM (G13XX)		
Data Lines (G131X)	16	A6
Address/Data (G132X)	16	A6
Timers (G14XX)		
Timer 2 (G141X)	16	A7
DMAs (G15XX)		
DMA 0 (G151X)	16,17	A7
DMA 1 (G152X)	16,17	A7
Mesg Intrfce (G16XX)		
Data (G161X)	20	A7
Address/Tag (G162X)	20	A7
Timebases (G2XXX)		
Clocks (G21XX)		
20.0000 MHz (G211X)	14	A5
19.6608 MHz (G212X)	10	A5
Main (G22XX)		

Circuits Not Covered by Diagnostic Tests

The following list shows those circuits and boards in the 11401/402 Digitizing Oscilloscope mainframe which are less than 50% functionally verified (directly or indirectly) by the Extended Diagnostics menus tests. Boards and circuits not on this list are 50 to 100% functionally tested by the Diagnostic tests with or without installed plug-in units. Before testing, install three, 11K generic plug-in amplifiers (i.e., 11A32, 11A34, 11A52) to ensure good functional verification of the Digitizer subsystem. Entries that depend on installed plug-in units for proper testing include the phrase "with plug-in units" with the degree of coverage. Functional verification is 0% unless the item is classified as "partial", in which case it is 1-50% tested. Numbers within "<>" indicate the associated schematic numbers.

Refer to the Cabling Diagram, schematic <42>, for the schematic diagrams that correspond to each board.

List of Circuits Not Fully Covered by Diagnostic Tests

Plug-in Interface Board—Partial with plug-in units.

Acquisition Board

- Acq Sampler <6>
  - Sample Gate Generator—Good with plug-in units.
  - Strobe Generator—Good with plug-in units.
  - Strobe Driver—Good with plug-in units.
  - Sampler—Good with plug-in units.
  - Vertical Channel Select—Good with plug-in units.
- Acq Clock Generators & Time Interpolators <7>
  - Fine Time Interpolators
  - Fine Time Interpolators Mux
  - Fine Time Interpolators Shift Register
  - Course Time Interpolators
  - Course Time Interpolators Mux
- Acq Trigger & Holdoff Logic <10>
  - Trigger Source Register—partial
  - Trigger Signal Buffers

Trigger Hybrid—partial

Buffer—partial

Trigger Signals Conditioner—partial

Delay By Events—partial

Holdoff Logic—partial

Acq Main & Window Fine Holdoff Generators <11>

Acquisition Control Register—partial

Main Fine Holdoff Generator

Window Fine Holdoff Generator

Acq Autocal & Refresh <12>

Plug-in Ground Select—Good with plug-in units.

Timebase Board

TB A/D Interface & System Clock <14>

Invalid Point Detect

TB Control Latches & Plug-in Sequencer <15>

Timebase Status Readback Buffer—partial

Last Request Control—partial

Chop Controller & Plug-in Sequencer—partial

Chop Transition Blanking—partial

Aux Z-Axis Blanking

TB MPU Kernel & Address Decoding <16>

Wfm ID Tables Select—partial

TB Main Counters <18>

Main Request Logic

Last Request Generation

Window 2 Seek Control

Window 2 Request Logic

TB Window Counters <19>

Window 1 Seek Control

Window 1 Request Logic

TB DAG Interface <20>

Final Wfm ID Encoding Table—partial

Destination Address Generator—partial

Restart Control—partial

Rear Panel Board

Rear Panel—GPIB & RS-232-C <3>

GPIB Controller—partial

GPIB Data Buffers

GPIB Control Driver

GPIB Status

I/O Board

I/O-Internal & Control <21>

Real Time Decode/Request—partial

Realtime Clock—partial